AFIT/GE/ENG/99M-25

MODULATION OF ELECTROSTATIC MICROELECTROMECHANICAL MIRRORS USING A CMOS CONTROLLER

THESIS

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AFIT/GE/ENG/99M-25

REPORT DOCUMENTATION PAGE	Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	8 Mar 99	Master's Thesis Sep 98-Mar 99

4. TITLE AND SUBTITLE
MODULATION OF ELECTROSTATIC MICROELECTROMECHANICAL MIRRORS USING A CMOS CONTROLLER

5. FUNDING NUMBERS

6. AUTHOR(S)
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AFIT/GE/ENG/99M-25

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10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
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12a. DISTRIBUTION AVAILABILITY STATEMENT
Distribution Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

Microelectromechanical Systems (MEMS) is a rapidly growing technology that lends itself particularly well to optical applications. An example of an optical MEMS device is the piston-action mirror that modulates the phase of reflected light. The phase of reflected light can be varied using thermal or electrostatic actuation to control the position of the mirror. In previous research, a modulation method to control thermally actuated mirrors was developed.

This thesis presents the development, implementation, fabrication, and testing of a complimentary metal oxide semiconductor (CMOS) controller capable of directly interfacing between a digital system, such as a computer, and an electrostatically actuated MEMS mirror device. The controller pulse width modulates a supply voltage to vary the power applied to the MEMS mirror device. The MEMS mirror device responds with negligible position ripple to the applied average power of the pulse width modulation signal. By varying the duty cycle of the pulse width modulation signal, the position of the mirror is varied. This controller can be adapted to control other electrostatically actuated devices using the design and methodology described in this thesis. The implementation of this controller is a step toward the monolithic integration of a MEMS deformable mirror array with CMOS control electronics.

14. SUBJECT TERMS
micromirror devices, micromachining, MEMS, MUMPs, micromechanical, flexure-beam, interferometer, electrostatic actuation, pulse width modulation, VLSI

15. NUMBER OF PAGES
103

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

AFIT/GE/ENG/99M-25

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THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
Air Education and Training Command
In Partial Fulfillment of the Requirements for the
Degree of Master of Science

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March 1999

AFIT/GE/ENG/99M-25

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Acknowledgments

This thesis is the combined effort of many individuals, despite the fact that my name appears alone on the cover sheet. To begin, I would like to thank my savior, Jesus Christ, and his massive support organization including the Apex ministry at Far Hills Baptist Church and the BASIC ministry at Fairhaven Christian and Missionary Alliance Church. These programs gave me the spiritual, emotional, and social support that I needed to endure my time at AFIT.

Secondly, I thank my family for all the encouragement and love I have received. You have always supported me in all my endeavors. You provided for me and made many sacrifices so that I could be better equipped to succeed in life. Thank you for all your support and love.

Next, I would like to thank my sponsor for funding my research, Major John H. Comtois, Ph.D. at ARFL/VSSE. In addition, my committee, Major Charles P. Brothers, Ph.D., Major James A. Lott Ph.D., and Captain Jeff T. Butler, Ph.D., continuously and not always gently prompted me along the path to completion of this research and deserve a great deal of thanks for tolerating me.

Finally, I would like to thank my fellow AFIT students in the VLSI lab. We suffered through many long days and late nights together, but your friendship helped make the time bearable. I would like to especially thank Captain David J. Barnhart, my fellow VLSI guy. Your humor and optimism made working the lab almost enjoyable (I should emphasize almost). Thank you, good luck, and best wishes to all who made this work possible.

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Abstract

Microelectromechanical Systems (MEMS) is a rapidly growing technology that lends itself particularly well to optical applications. An example of an optical MEMS device is the piston-action mirror that modulates the phase of reflected light. The phase of reflected light can be varied using thermal or electrostatic actuation to control the position of the mirror. In previous research, a modulation method to control thermally actuated mirrors was developed.

This thesis presents the development, implementation, fabrication, and testing of a complimentary metal oxide semiconductor (CMOS) controller capable of directly interfacing between a digital system, such as a computer, and an electrostatically actuated MEMS mirror device. The controller pulse width modulates a supply voltage to vary the power applied to the MEMS mirror device. The MEMS mirror device responds with negligible position ripple to the applied average power of the pulse width modulation signal. By varying the duty cycle of the pulse width modulation signal, the position of the mirror is varied. This controller can be adapted to control other electrostatically actuated devices using the design and methodology described in this thesis. The implementation of this controller is a step toward the monolithic integration of a MEMS deformable mirror array with CMOS control electronics.

MODULATION OF ELECTROSTATIC MICROELECTROMECHANICAL MIRRORS USING A CMOS CONTROLLER

1 Introduction

1.1 Background

This research is an outgrowth of previous research conducted at the Air Force Institute of Technology. In the previous research, thermally actuated Micro-electromechanical System (MEMS) mirrors were controlled by using various modulation methods. It was theorized that similar modulation methods could be applied to electrostatic MEMS mirror devices [1]. The goal of this research was to develop a modulation method capable of controlling MEMS electrostatic devices, and to design, fabricate, and test a single-chip complimentary metal oxide semiconductor (CMOS) controller capable of efficiently controlling an array of MEMS electrostatic mirror devices.

1.2 Problem Statement

The integration of MEMS and CMOS devices is a rapidly growing field of research with many problems yet to be solved. MEMS and CMOS circuits may be integrated in a variety of ways including: monolithic fabrication, multichip modules, and

separately packaged devices connected by external means. Researchers are attempting to solve the problems associated with the incompatible foundry fabrication processes of MEMS and CMOS. By tightly integrating CMOS and MEMS processing, a relatively low-weight, low-cost, high performance product can be produced [1].

The purpose of this research is to develop, implement, fabricate, and test a multi-channel controller capable of positioning individual MEMS mirrors in an array. The role of the CMOS controller is shown in Figure 1-1.

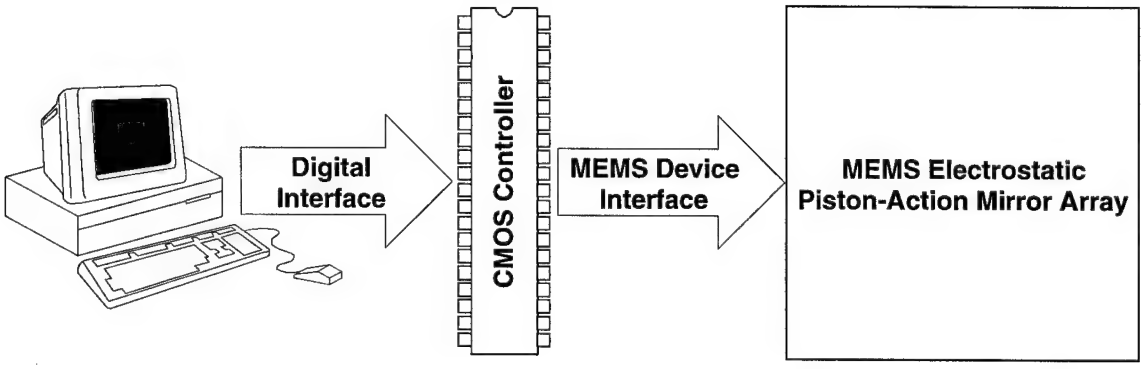

Figure 1-1. System Level Diagram.

Using the MEMS device interface, the CMOS controller must be capable of fully controlling the position of each MEMS mirror independent of the position of every other mirror. The implication of this approach is that each mirror must be individually addressable and that the CMOS controller must have a dedicated channel for each mirror. In addition, the controller must interface with the MEMS mirrors with a minimal amount of hardware external to the CMOS controller.

The CMOS controller must connect directly to a digital control system, such as a computer, through the digital interface. As with the MEMS device interface, the digital interface must be implemented with a minimum amount of overhead logic. Although the

CMOS controller demonstrated in this thesis is an all-digital CMOS design that is fabricated and packaged separately from the MEMS mirror devices, its design is targeted for implementation in either a multi-chip module or monolithic CMOS-MEMS fabrication process.

1.3 Methodology

The overall research was organized into five milestones that advanced the research from concept to testing. The first milestone was a theoretical investigation of the MEMS mirror devices to be controlled. This included both a steady state model and a frequency response model describing the operation of the MEMS device under control.

The second milestone was accomplished when pulse width modulation was chosen as the modulation method to be implemented. Several modulation methods used to control the MEMS mirror devices were investigated. The modulation method must compliment the frequency response model and be compatible with the steady state model. In addition, the modulation method should be transparent to the operation of the device and mimic the steady state control of the mirror devices. Pulse width modulation was chosen and investigated through modeling and experimental measurements.

The implementation of the controller was the third milestone and included MEMS mirror-imposed design constraints and fabrication process-specific design constraints. The intended adaptive optics application required the MEMS mirror to be controlled with at least a 3-bit resolution. An 8-bit resolution was chosen to exceed the minimum requirements and to be more compatible with a standard digital interface. The MEMS mirrors also imposed a minimum refresh frequency to reduce position variations of the

MEMS mirrors. A 1.2 μm CMOS fabrication process was targeted. The 1.2 μm CMOS process provided a standard 40-pin dual inline package (DIP) pad frame and was compatible with the available design tools and standard cell libraries. The standard pad frame specified the maximum available die area for the circuit logic and the number of input and output pins. The fabrication of the CMOS controller was the fourth milestone.

The fifth and final milestone was the testing and demonstration of the CMOS controller. Testing consisted of preliminary verification inspections of the CMOS controller and two functional operation experiments. The CMOS controller demonstration consisted of two sets of measurements, a baseline measurement using the existing laboratory test setup and a measurement using the CMOS controller. The baseline measurements were performed using the known steady state control method. Measurements of the same device were repeated using the CMOS controller. The results of the two sets of measurements were analyzed and compared.

1.4 Overview

The information presented here in Chapter 1 is expounded upon in the following six chapters. Chapter 2 includes a review of the current literature relevant to the design, fabrication, and operation of MEMS electrostatic mirrors, specifically flexure beam mirror devices. In addition, theories describing the frequency response of the MEMS mirrors and the pulse width modulation method are discussed.

Chapter 3 contains the top-level design of the CMOS modulation controller. Specifically, the high-level design issues imposed by the mirror devices upon the CMOS

design are covered. In addition, the very large scale integration (VLSI) design considerations are prioritized, and the design constraints are established.

The top-level CMOS controller design presented in Chapter 3 is implemented using standard cell libraries and compatible design tools, as described in Chapter 4. The entire CMOS controller design is segmented into small functional blocks. A description of the function of each block and the interconnectivity of the blocks are given in Chapter 4. In addition, the fabrication process, standard cell libraries, and design tools are discussed in Chapter 4.

The experiments used to determine the performance of the controller design are explained in Chapter 5. The first set of experiments describes the process used to verify the correct operation of the CMOS controller. The second set of experiments determines the modulation performance of the CMOS controller.

The results of the experiments described in Chapter 5 are presented in Chapter 6. A design error was found in the CMOS controller that required permanent modification to correct. Also in Chapter 6, the performance of the controller is compared a conventional test setup.

Chapter 7 includes a summary of the information presented in Chapters 1 through 6. In addition, conclusions derived from this research and areas for improvement of the CMOS controller that will enable integration into a multichip package or monolithic CMOS-MEMS fabrication process are discussed. Further areas of research derived from this thesis are enumerated in Chapter 7.

2 Literature Review

2.1 Introduction

An understanding of electrostatic microelectromechanical (MEMS) mirror devices, their operation, and their construction is necessary in order to develop a complimentary metal oxide semiconductor (CMOS) controller capable of modulating these mirrors. The primary components of electrostatic piston-action mirrors and a typical mirror example, the flexure beam mirror device (FBMD), are described in Section 2.2. The ideal modeling of the FBMD presented in Section 2.3 provides a mathematical relationship between control voltage and FBMD deflection. The control voltage for electrostatic FBMDs is currently provided by a static voltage source, either a variable power supply or a digital-to-analog converter (DAC), as discussed in Section 2.4. Modulation methods used to control thermal MEMS devices are also included in Section 2.4. The fabrication process used to produce the FBMDs is illustrated in Section 2.5 with a FBMD pictorial guide to the Microelectronic Center of North Carolina's Multi-User MEMS Process (MUMPs). The theoretical frequency response of the FBMDs presented in Section 2.7 predicts that the position response of the FBMDs continually decreases as the frequency increases above the resonant frequency.

In addition to understanding the electrostatic MEMS mirrors and their operation, the modulation technique used in this thesis must be understood in order to properly control the mirror devices. This modulation technique, pulse width modulation, is described in Section 2.6.

2.2 Electrostatic Piston-Action Mirrors

Electrostatic piston-action mirrors consist of a movable mirror, a suspension system, an addressing electrode, and a dielectric medium between the mirror and the electrode. A Cartesian coordinate system is used to describe all forces and geometries of the FBMD. The substrate of the wafer, the mirror, and the address electrode lie in the X-Y plane with the Z-axis orthogonal to the surface of the wafer, as shown in the schematic representation of the FBMD in Figure 2-1 [2].

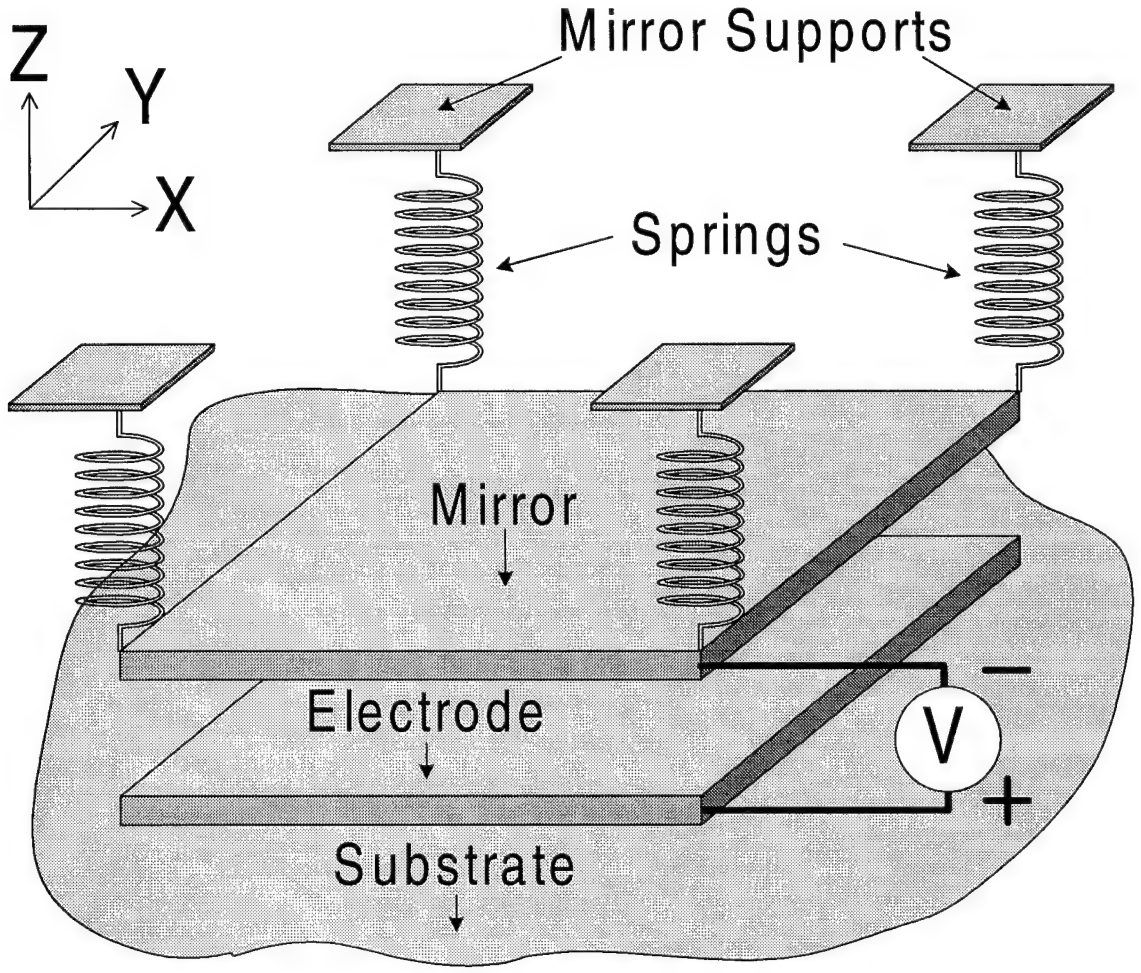

Figure 2-1. Schematic Representation of an Electrostatic Piston-Action Mirror.

The mirror moves along the Z-axis, as the name piston-action implies. A set of springs connecting the mirror to a series of mirror supports comprises the suspension system. By suspending the mirror above the electrode with the springs, the mirror is allowed to travel in the Z direction. The potential difference applied between the mirror and the electrode, opposed by the force of the springs, controls the distance of the mirror above the electrode [2].

A typical example of an electrostatic piston-action mirror is depicted by the FBMD design shown in Figure 2-2. Both a top and a side view of the FBMD are shown. The flexures are rigid and resist deformation, thus performing the function of the springs illustrated in Figure 2-1. The flexure design limits the motion of the mirror to the Z direction, with negligible motion in the X or Y directions [2].

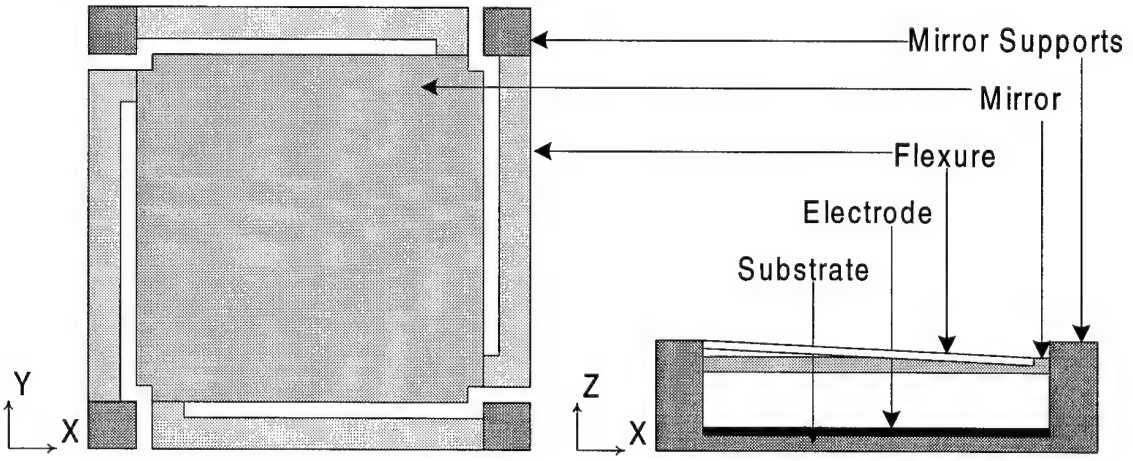

Figure 2-2. Top and Side view of a Flexure Beam Mirror Device.

2.3 Static Operation of Flexure Beam Mirror Devices

The analysis of the ideal operation of the FBMD presented in this section is based on the static balancing of all forces acting on the mirror [2]. Figure 2-3 illustrates several variables necessary to further explain the operation of the FBMD.

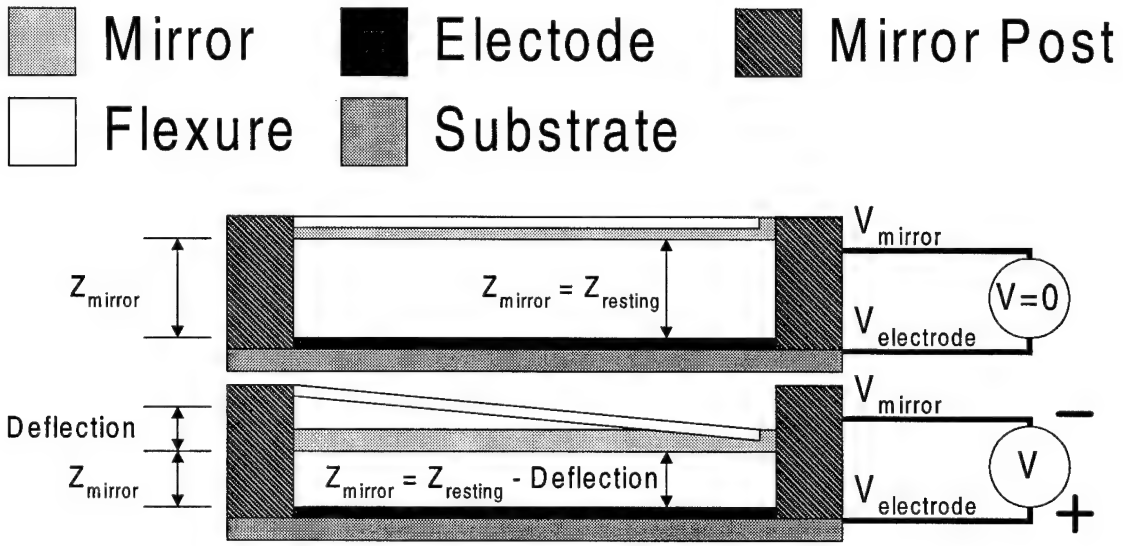

Figure 2-3. FBMD Variables Definition Schematic.

The potential difference between the electrode and mirror is defined as V. Z_{mirror} describes the height of the mirror above the electrode. Z_{mirror} equals $Z_{resting}$ when no potential difference is applied (V equals zero). *Deflection* is the measure of the deviation of the mirror from its resting height $Z_{resting}$. The dielectric medium in the volume bounded between the mirror and the electrode has a dielectric constant, ε, which depends upon the operational environment of the mirror. The following model considers only two forces acting on the mirror: the force of the flexures $F_{flexure}$ and the electrostatic force

$F_{electrostatic}$. To simplify the math and the construction of the device, the electrode and the mirror are assumed to have the same surface area, A [2].

The first force acting upon the mirror is the electrostatic force. This force is described by Equation (2-1) [3].

$$F_{electrostatic} = -\frac{A \cdot \varepsilon \cdot V^2}{2 \cdot Z_{mirror}^{\ 2}} \tag{2-1}$$

The second force acting on the mirror is the restoring force of the flexures. These flexures operate as springs and are subject to Hooke's Law [4]:

$$F_{flexure} = k \cdot Deflection \tag{2-2}$$

where k is the spring constant. For flexure springs, the spring constant k is modeled as [5]:

$$k = n \cdot \left[\frac{E \cdot w \cdot t^3}{L^3} + \frac{\sigma \cdot (1-\upsilon) \cdot w \cdot t}{2 \cdot L} \right] \tag{2-3}$$

where n is the number of flexures, w, L, and t are the width, length and thickness of the flexure, respectively, and E, σ, and υ are the residual stress, the modulus of elasticity, and the Poisson ratio of the flexure material, respectively. When the mirror is not moving, Newton's First Law is valid and [4]:

$$\sum F = 0 = F_{flexure} + F_{electrostatic} \tag{2-4}$$

Expanding Equation (2-4) with Equations (2-1), (2-2), and (2-3) yields:

$$\frac{A \cdot \varepsilon \cdot V^2}{2 \cdot Z_{mirror}^{\ 2}} = n \cdot \left[\frac{E \cdot w \cdot t^3}{L^3} + \frac{\sigma \cdot (1-\upsilon) \cdot w \cdot t}{2 \cdot L} \right] \cdot Deflection \tag{2-5}$$

Solving Equation (2-5) for V and relating Z_{mirror} to *Deflection* as shown in Figure 2-3, the voltage necessary for a given deflection is [2]:

$$V = \left(Z_{resting} - Deflection\right) \cdot \sqrt{\frac{2 \cdot Deflection}{\varepsilon \cdot A} \cdot n \cdot \left[\frac{E \cdot w \cdot t^3}{L^3} + \frac{\sigma \cdot (1-\upsilon) \cdot w \cdot t}{2 \cdot L}\right]} \qquad (2\text{-}6)$$

Despite the appearance of complexity, Equation (2-6) is very simple since every variable, except *Deflection*, reduces to a constant for a given mirror. Examples of the model simplification are shown in Chapter 6.

Equation (2-6) models the position of the mirror only for *Deflections* below approximately one third the gap between the mirror and the address electrode. For *Deflections* greater than one third of the gap, the mirror position becomes unstable causing the mirror to contact the address electrode, an effect called "snap through instability" or "snap-down". This effect is believed to be caused by the fact that the electrostatic force increases much more rapidly than the restoring spring force as *Deflection* increases [6].

2.4 Current Flexure Beam Mirror Device Control

Currently discrete digital-to-analog converters (DACs) are used to provide the control voltage to the FBMDs. However, these DACs are limited in the voltage range that can be produced, usually below ten volts. To increase the *Deflection* range, an additional power supply is connected between the FBMDs control nodes and the DAC output to offset the control voltage. The control voltage becomes the sum of the power supply voltage and the DAC output. Because the *Deflection* is proportional to the square of the control voltage, offsetting the control voltage produces a larger range of

Deflections. However, in this configuration, the total usable *Deflection* range is decreased from the possible *Deflection* range modeled with Equation (2-6) [7].

Subsequent research has shown that thermal actuators respond to the average power of a control signal if the control signal's period is much less than the mechanical time constant of the actuator. Using pulsed inputs of varying amplitude or varying frequency, thermal actuators were controlled without DACs. This research also theorized that such modulation methods could be adapted to electrostatic devices [1]. Sections 2.6 and 2.7 discuss the details of the modulation method and frequency response for electrostatic devices.

2.5 Surface Micromachining of Flexure Beam Mirror Devices

The Microelectronics Center of North Carolina fabricated all the FBMDs utilized in this research using MUMPs. MUMPs is a surface micromachining process consisting of three polysilicon structural layers and two sacrificial layers[1] [8]. Surface micromachining is a process that uses thin-film deposition and photolithographic layer masking and etching. A unique capability of surface micromachining is the use of sacrificial layers that allow the structural material to be either suspended or free-floating [1]. After all layers have been deposited, a release etch is performed to remove the sacrificial layers [8]. The remainder of this section will describe a FBMD design fabricated using the MUMPs process.

---

[1] Sacrificial layers - layers which are removed from the final product and used as forms and/or spacers for the structural layers.

To begin, an initially n-type (100) silicon wafer is doped with phosphorus to achieve 1-2 Ω-cm resistivity to reduce charge buildup between the substrate and the polysilicon structural layers. Next, a 600 nm layer of silicon nitride is deposited over the entire surface of the wafer using low-pressure chemical vapor deposition (LPCVD). This layer electrically isolates subsequent layers from the substrate and is not patterned. A 500 nm layer of polysilicon is then deposited on top of the silicon nitride as shown in Figure 2-4. This polysilicon layer is referred to as Poly0 [8].

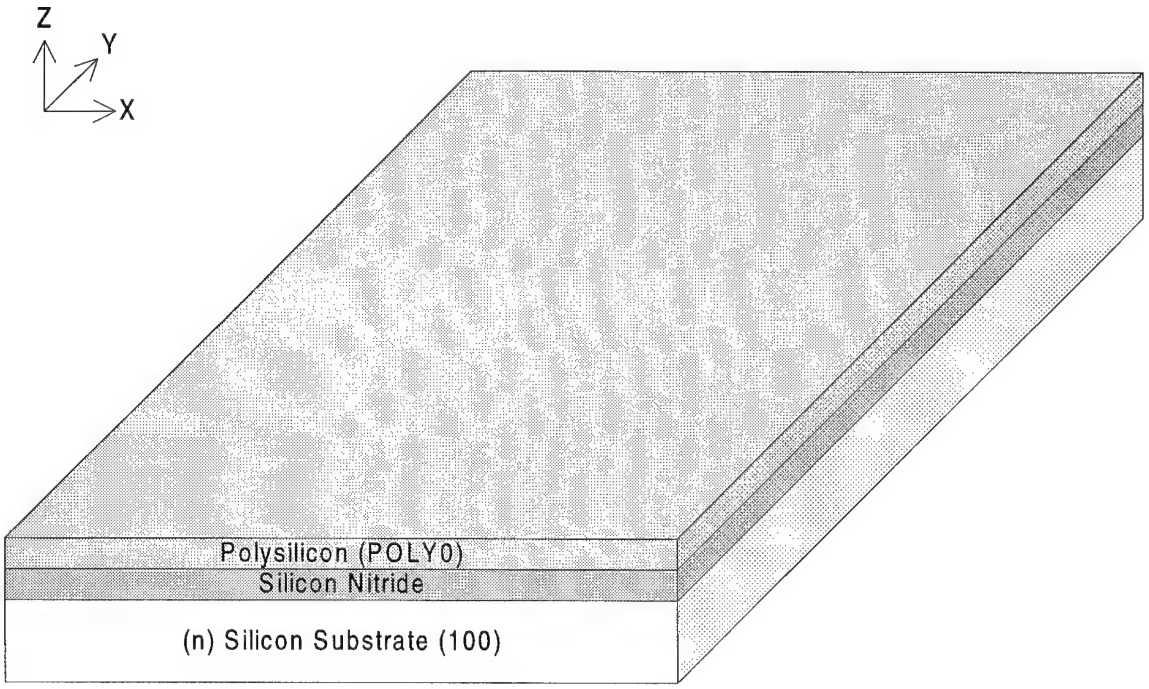

Figure 2-4. Initial Depositions over the Entire Substrate.

Since Poly0 is a patternable layer, selected areas of Poly0 are removed as specified by the designer. This material removal is accomplished using photolithography and etching processes similar to those found in the integrated-circuit industry [8].

The patterned Poly0 layer is displayed in Figure 2-5. The large structure in the center is the address electrode. The four smaller structures around the address electrode are the mirror support bases.

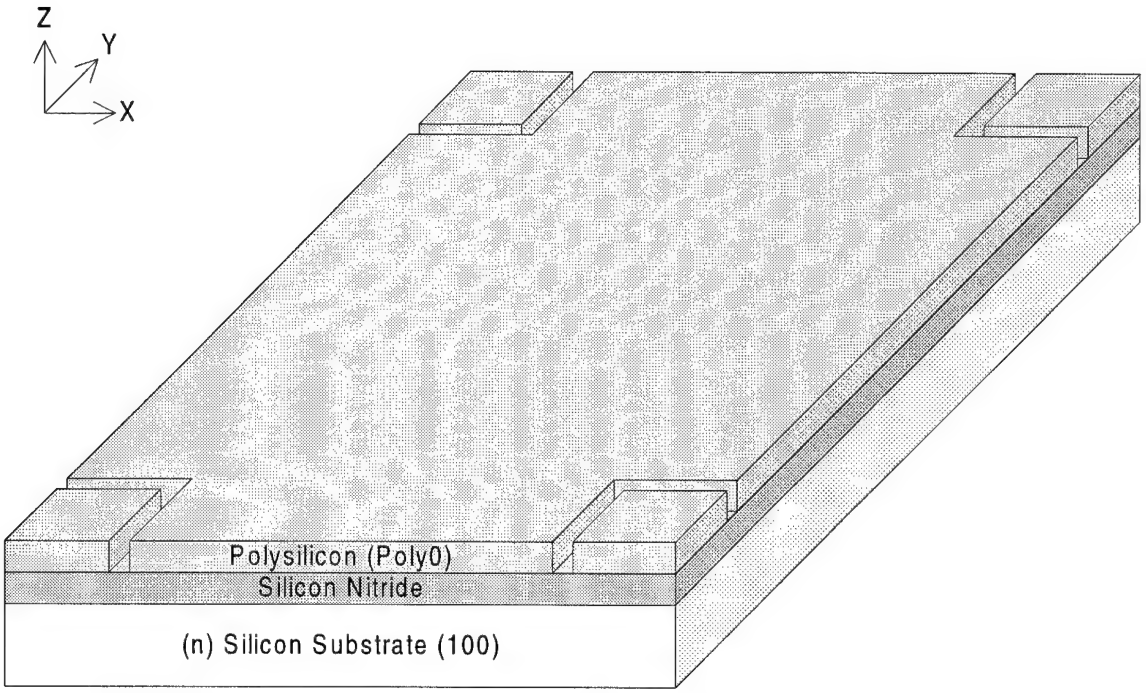

Figure 2-5. Poly0 Mirror Supports and Address Electrode.

Once the Poly0 has been patterned, a 2 μm sacrificial layer of phosphosilicate glass (PSG) named Oxide1 is deposited via LPCVD. The Oxide1 separates the structural layers Poly0 and Poly1. The Oxide1 also determines the shape of Poly1's lower surface. After the Oxide1 deposition, a partial etch specified by another designer-defined pattern, labeled Dimple, is accomplished [8]. The Dimple areas produce a small protrusion on the lower side of Poly1 which reduces the sticking effect between Poly0 and Poly1 structures upon contact by decreasing the contact surface area [6].

The Dimple shapes are etched into Oxide1 to a depth of 750 nm [8]. Figure 2-6 shows the result of all previous processing steps and a detailed view of the Dimple etch.

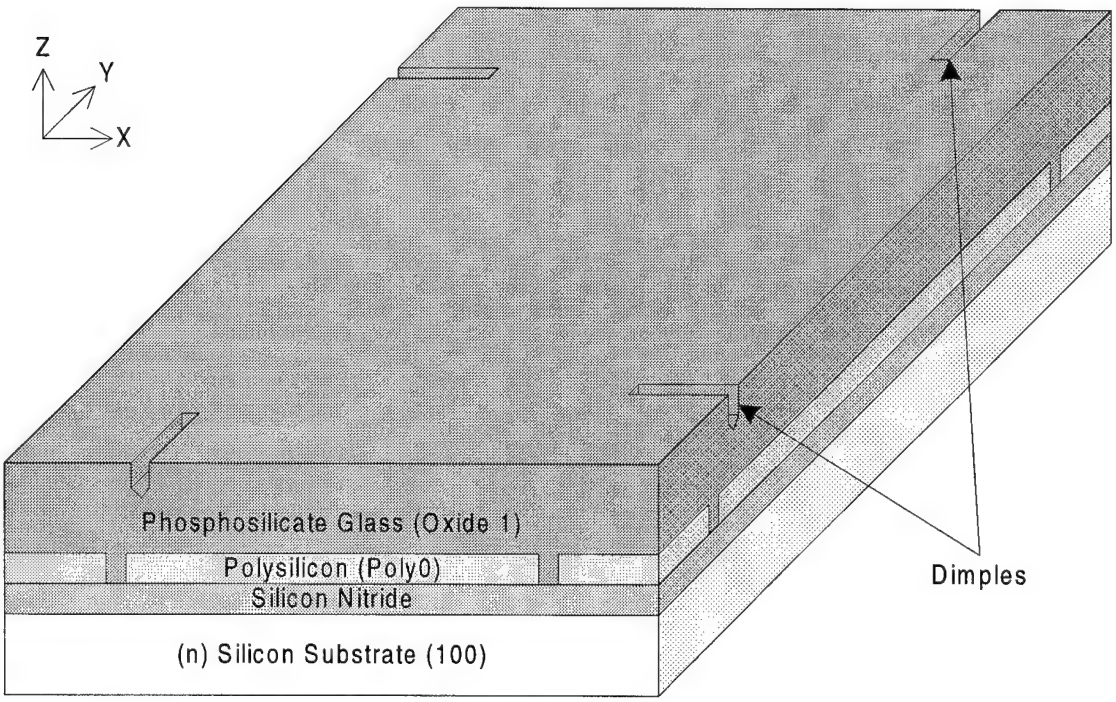

Figure 2-6. Oxide1 and Dimple Processing Results.

Following the Dimple operation, an etch is performed to remove designer-selected areas of Oxide1. The designer-selected removal patterns, titled Anchor1, selectively removes all of Oxide1 down to the Poly0 so that the surface of the Poly0, under the Anchor1 areas, is exposed as illustrated in Figure 2-7. These exposed areas of the Poly0 will directly contact the second polysilicon layer, Poly1. The etched Anchor1 areas shape the Poly1 mirror supports when Poly1 is deposited [8].

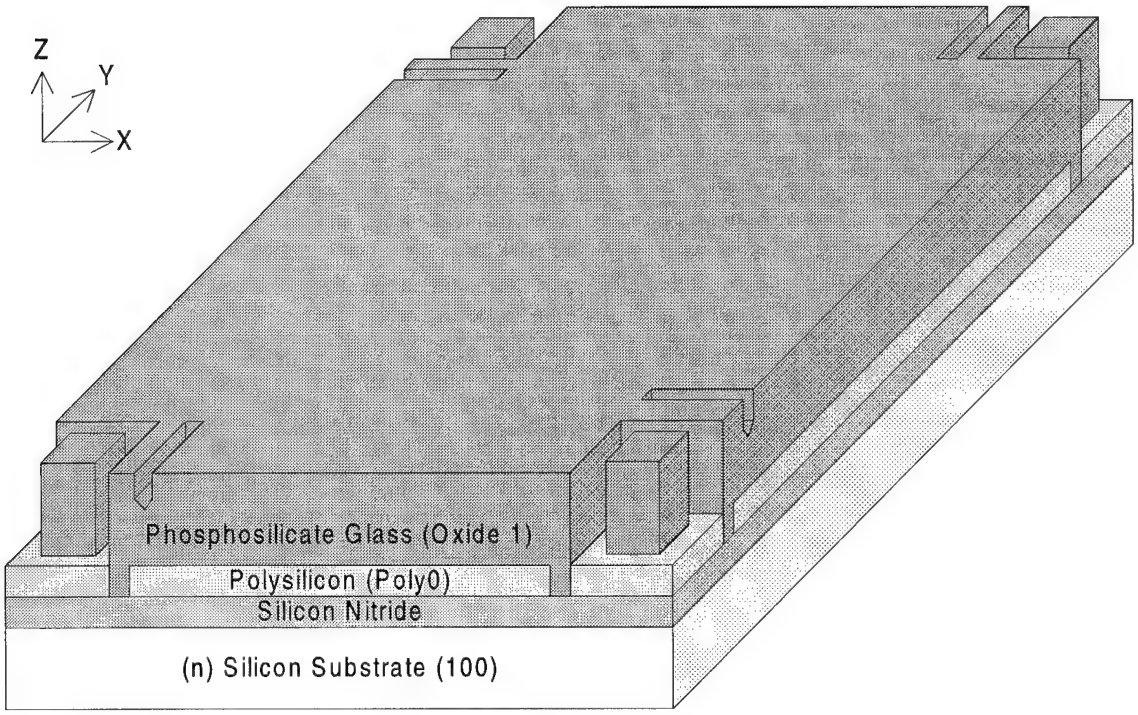

Figure 2-7. Anchor1 Etch into Oxide1.

After the Anchor1 etch, the Poly1 layer is deposited by LPCVD to a thickness of 2 μm. Like Poly0, designer-defined areas of Poly1 are removed using the patterning operations described previously. The remaining Poly1 area is shown in Figure 2-8. The large area in the center of the structure is the mirror base and has the same shape as the electrode shown in Figure 2-5. Attached to the mirror base are four L-shaped flexures, one on each side of the mirror. Attached to the opposite end of each flexure is a mirror support. Because the Anchor1 etch removed any barriers between Poly0 and Poly1, the mirror supports are firmly joined to the Poly0 mirror support base [8].

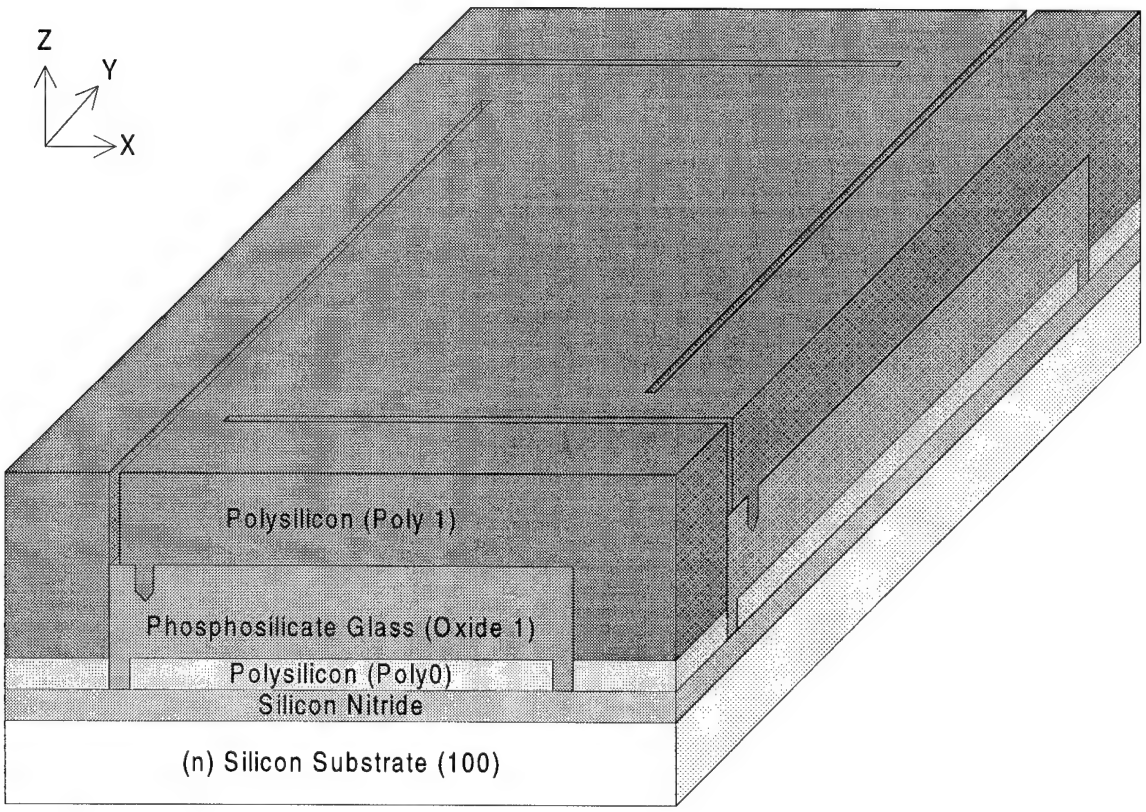

Figure 2-8. Poly1 Flexures, Mirror Base, and Mirror Supports.

After Poly1 is shaped, another PSG layer, Oxide2, is LPCVD deposited 750 nm thick. Similar to Oxide1, Oxide2 is patterned with an etching process. A selective etch removes all of Oxide2 down to Poly1 from designer-specified areas called Poly1Poly2Via, as exhibited in Figure 2-9 [8].

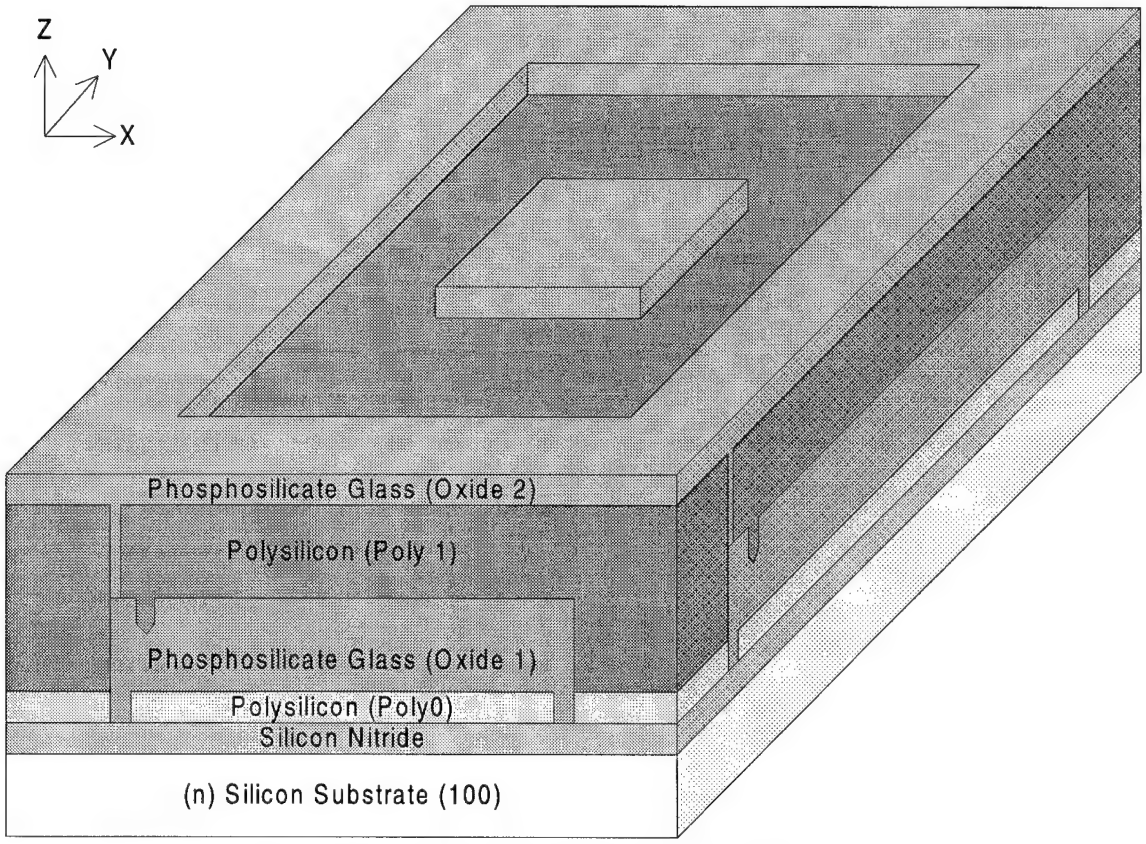

Figure 2-9. Poly1Poly2Via and Oxide2 Processing.

After Oxide2's deposition and shaping, a 1.5 μm thick polysilicon layer called Poly2 is then deposited. The Poly2 is anchored to Poly1 where Oxide2 was removed [8]. This Poly1 and Poly2 anchoring structure is referred to as "stacked poly". Notice the remaining center rectangle of Oxide2 in Figure 2-9. This is referred to as "trapped oxide" because the oxide is completely enclosed between surrounding layers of polysilicon.

When the device is released, the exposed areas of both Oxide1 and Oxide2 layers are removed. The "trapped oxide" remains because the etchant does not penetrate the encapsulating polysilicon [9]. Because Poly2 is deposited then selectively removed by etching, both the Poly1 and Poly2 portions of the "stacked poly" structure will be shaped by the Poly2 shaping operation [8]. This effect cuts etch holes in the "stacked poly" mirror base. Figure 2-10 presents the result of the Poly2 deposition and shaping with etch holes cut through both the Poly1 and Poly2 layers. Removal of the sacrificial Oxide1 material would be very slow due to the relatively large size of the mirror and associated limited exposed surface area of Oxide1 underneath the mirror. Etch holes are added to increase the available surface area. This allows the release etchant additional paths to remove Oxide1 [8].

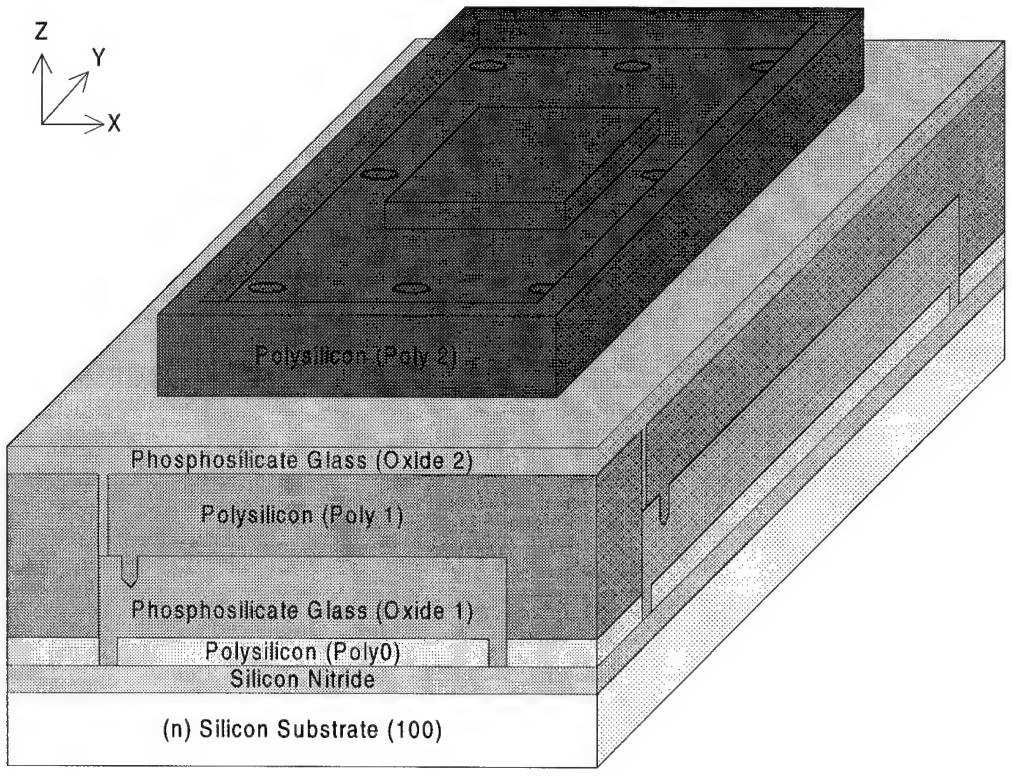

Figure 2-10. Poly2 Deposition and Shaping Results with Etch Holes.

The final deposition in the MUMPs process is a reflective gold mirror circle on top of the "trapped oxide" area of Poly2, as shown in Figure 2-11. The Metal layer is patterned using photolithography and a lift-off process. The use of gold increases the reflectivity of the mirror [8]. Table 2-1 summarizes the fabrication steps and their associated material layer thickness or material layer removal depth.

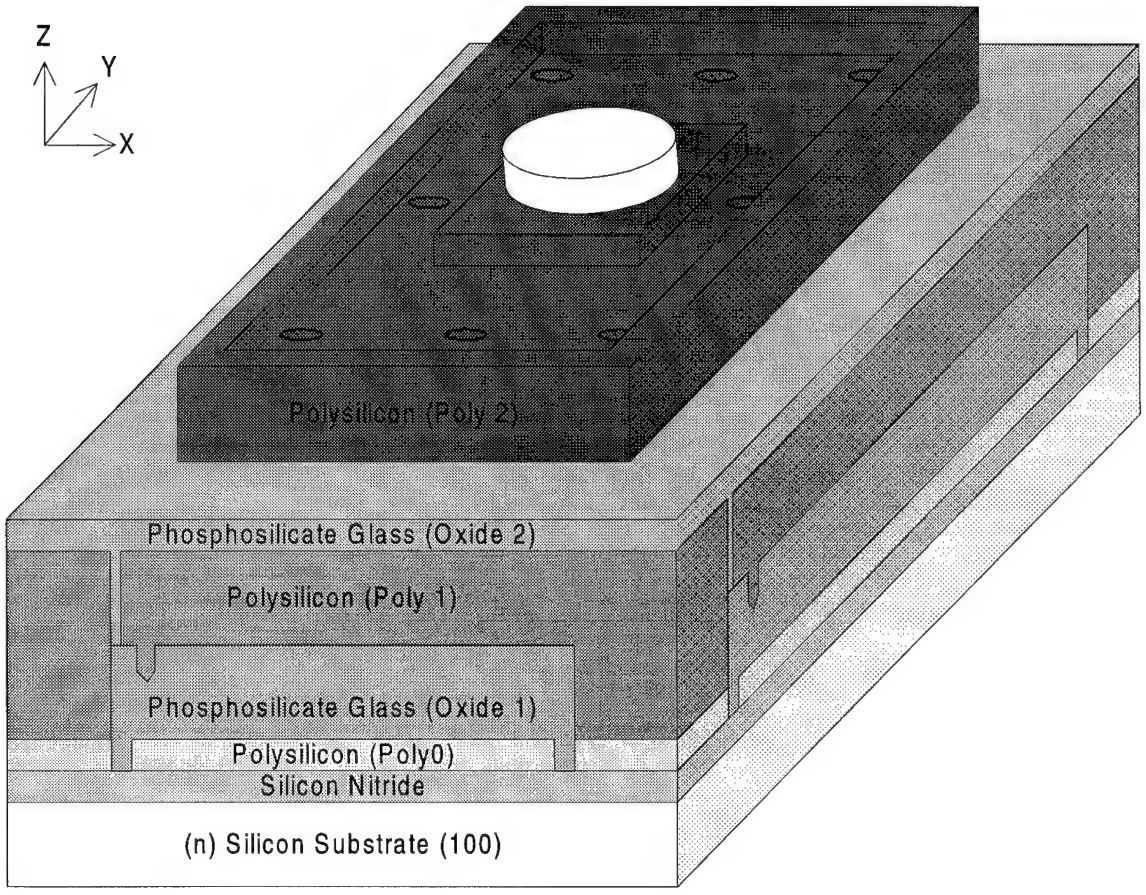

Figure 2-11. Gold Reflective Circle in Center of FBMD.

Table 2-1. Summary of MUMPs Fabrication Process Layer Thicknesses [8].

Fabrication Process	Thickness or Depth
Silicon Nitride	600 nm
Poly0	500 nm
Oxide1	2 μm
Dimple	750 nm
Anchor1	2 μm
Poly1	2 μm
Oxide2	750 nm
Poly1Poly2Via	750 nm
Poly2	1.5 μm
Metal	500 nm

Following the deposition and shaping of all the previously described layers, the device is submerged in a material-selective etchant. This etchant, usually diluted hydrofluoric acid, etches PSG much more rapidly than polysilicon. The device is placed in the etchant until all exposed sacrificial layers are removed. It is important to note that the structural polysilicon layers are etched, but much less rapidly than the PSG sacrificial layers. The actual material selectivity of the etch depends entirely upon the etchant being used and the temperature of the etchant [6]. Figure 2-12 displays a FBMD after release. To further illustrate the details of the FBMD example, Figure 2-13 reveals two cross-sectional views of the same FBMD design.

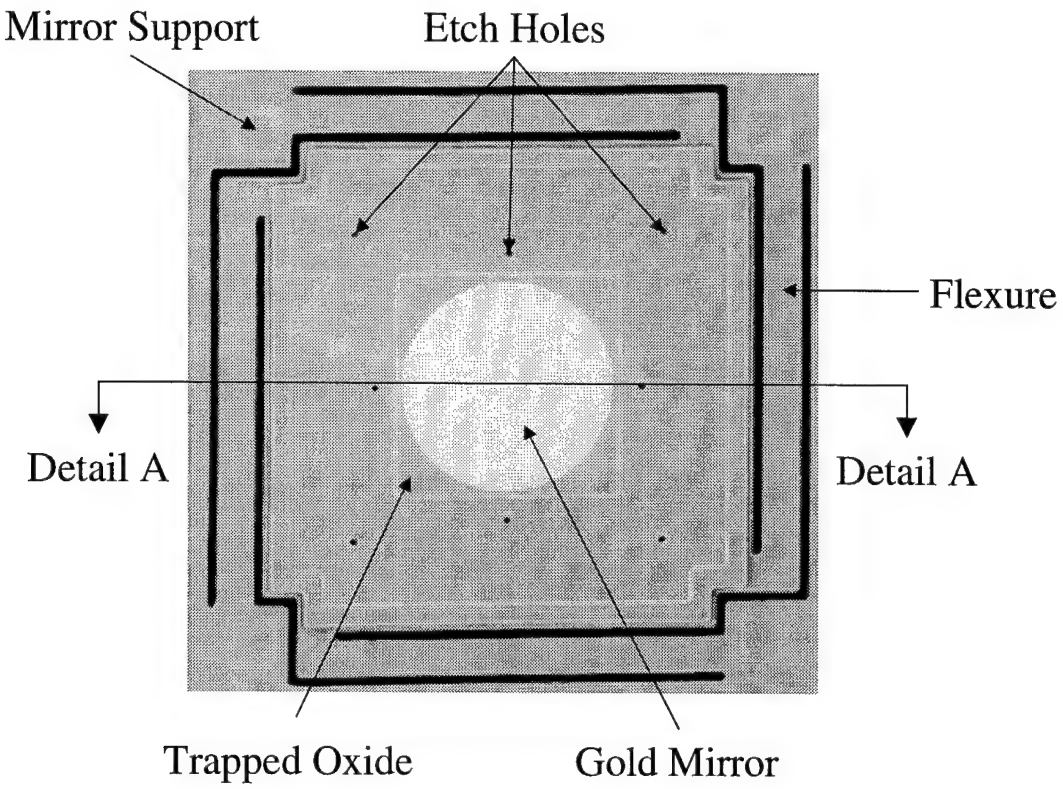

Figure 2-12. Scanning Electron Microscope View of FBMD [6].

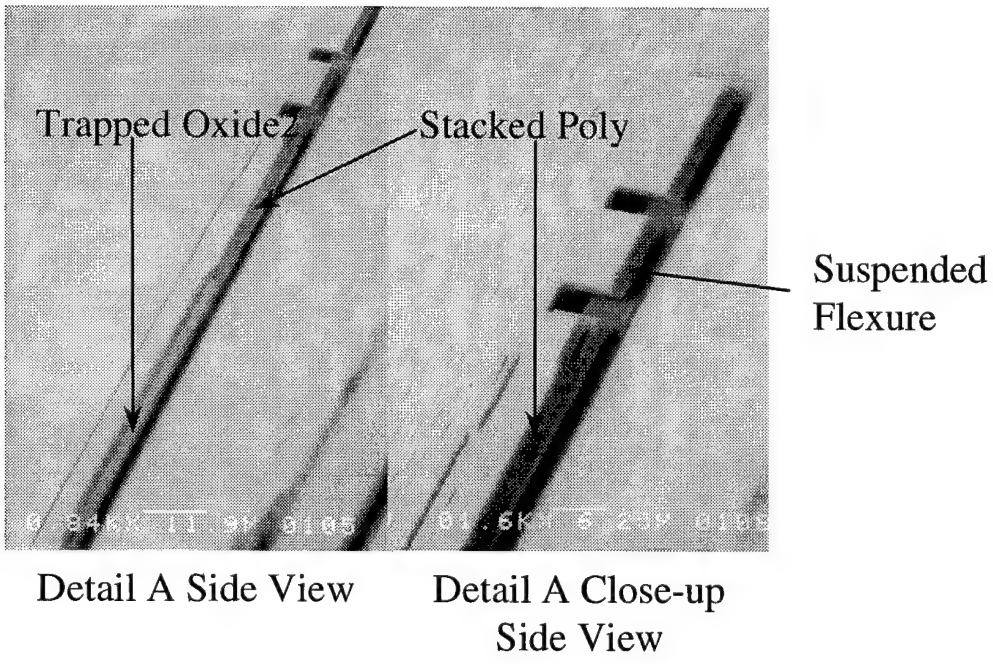

Figure 2-13. Cross-Section Views of FBMD.

2.6 Pulse Width Modulation

Pulse width modulation, when used as a voltage regulator, allows for the use of a single supply voltage, low complexity circuitry, high power efficiency, and ease of control. The pulse width modulator allows the output voltage to be some fraction of the supply voltage based upon the duty cycle. Thus, a single power supply can be regulated down to a lower voltage. The pulse width modulation regulator is relatively simple compared to other analog regulators, which may result in a smaller physical implementation when using a CMOS controller. In addition, the pulse width modulation regulator has an efficiency of greater than ninety percent, making the design ideal for low power applications [10]. The direct digital control eliminates the need for a complex digital-to-analog interface [1].

Pulse width modulation provides an average power transfer by varying the duty cycle of a square wave. In this application, a fixed supply voltage called the bias will be gated as shown in Figure 2-14.

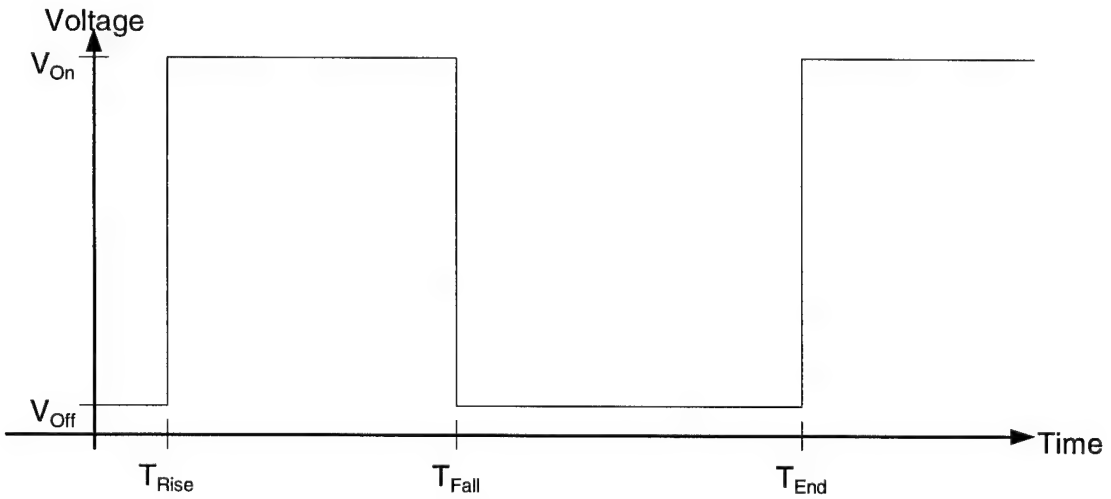

Figure 2-14. Pulse Width Modulation Variables Definition Waveform.

Applying the classic definition of root mean square voltage (Vrms) yields [11]:

$$Vrms = \left(\frac{1}{T} \cdot \int_{t}^{t+T} V(t)^2 \, dt \right)^{\frac{1}{2}} \tag{2-7}$$

where T is the period, t is any given time, and $V(t)$ is the instantaneous voltage at time t. Defining any rising edge T_{Rise} as the start of the periodic waveform and the next rising edge T_{End} as the end simplifies the mathematics. Expanding Equation (2-7) using the definitions shown in Figure 2-14 yields:

$$Vrms = \left(\frac{1}{T_{end} - T_{rise}} \cdot \int_{Trise}^{Tfall} (V_{On})^2 \, dt + \frac{1}{T} \cdot \int_{Tfall}^{Tend} (V_{Off})^2 \, dt \right)^{\frac{1}{2}} \tag{2-8}$$

which simplifies to Equation (2-9).

$$Vrms = \left(\frac{T_{fall} - T_{rise}}{T_{end} - T_{rise}} \cdot (V_{On} - V_{Off})^2 + (V_{Off})^2 \right)^{\frac{1}{2}} \tag{2-9}$$

Equation (2-10) defines the term duty cycle as relevant to Figure 2-14.

$$DutyCycle = \frac{T_{fall} - T_{rise}}{T_{end} - T_{rise}} \tag{2-10}$$

Power is defined as [11]:

$$Power = \frac{Vrms^2}{R} \tag{2-11}$$

where R is the resistance of the circuit being driven by the waveform. Substituting Equation (2-9) and (2-10) into Equation (2-11) simplifies to:

$$Power = \frac{DutyCycle \cdot (V_{On} - V_{Off})^2}{R} + \frac{(V_{Off})^2}{R} \tag{2-12}$$

Equation (2-12) reveals a linear relationship between power and duty cycle. Thus by varying the duty cycle, the amount of power delivered to the driven circuitry is varied. Although the pulse width modulated waveform is a time-varying signal, if the frequency of the waveform is much greater than the mechanical response of the driven device, the driven device will respond as if driven with a time-invariant signal of amplitude *Vrms*.

2.7 Frequency Response of Flexure Beam Mirror Devices

Since pulse width modulation uses time-varying signals, an analysis of the frequency response of the FBMD is necessary. Because the flexures act as springs, the FBMD resembles a harmonic oscillator. The equation for the response of a harmonic oscillator is [12]:

$$Z(t) = \frac{A \cdot \cos(\omega \cdot t)}{k - M \cdot \omega^2} \tag{2-13}$$

where k is the spring constant calculated in Equation (2-3), A is the amplitude of the driving force, ω is the frequency of the driving force, and M is the mass of the mirror. A graph of Equation (2-13), shown in Figure 2-15, demonstrates that frequencies greater than the resonant frequency are significantly attenuated and that the resonant frequency's theoretical amplitude approaches infinity at resonance.

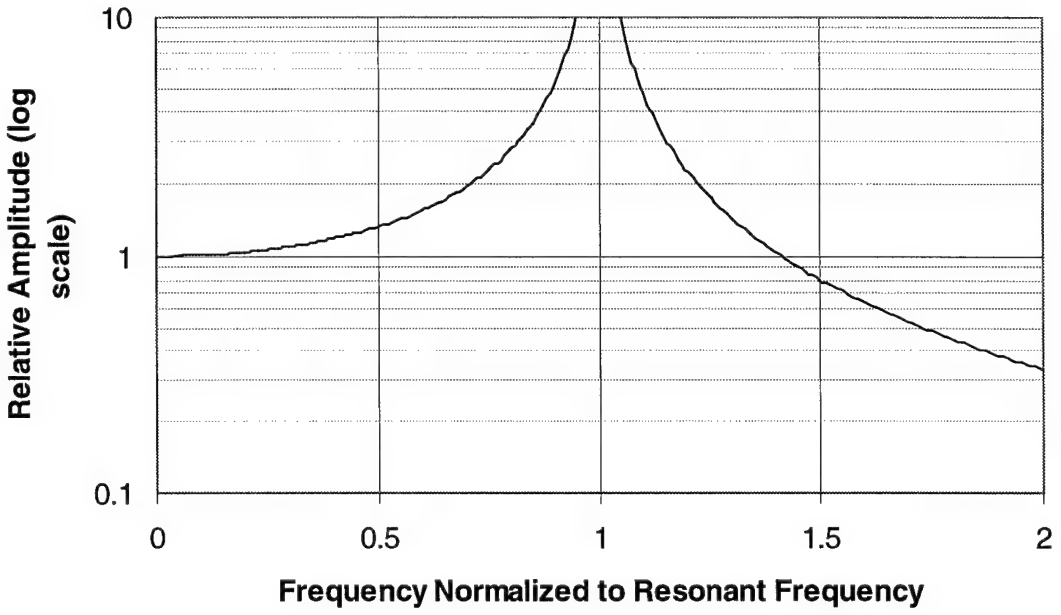

Figure 2-15. Mirror Deflection Response versus Normalized Frequency.

Solving for ω where Equation (2-13) is maximized, the resonant frequency is found to be [12]:

$$f_{resonant} = \frac{1}{2\pi} \cdot \sqrt{\frac{k}{M}} \tag{2-14}$$

where k is the spring constant defined by Equation (2-3) and M is the mass of the mirror

2.8 Summary

This chapter reviewed the design and operating theory of the FBMDs and the modulation theory employed in this research. By designing a pulse width modulator such that the lowest fundamental frequency of the waveform is greater than the resonant frequency of the mirror, the mirror should not respond directly to the stimulation

waveform. Instead, the response of the mirror should be proportional to the duty cycle of the stimulation waveform. The design of the controller is discussed in Chapter 3.

3 Design Requirements for the Mirror Controller

3.1 High-Level Design Issues

In a very large scale integration (VLSI) design, high-level design considerations imposed by the intended application of the design significantly influence several important design parameters, such as speed, performance, size, and power consumption. The electrostatic flexure beam mirror devices (FBMDs) described and modeled in Chapter 2 specify the minimum speed of the controller. Sections 3.2 and 3.3 analyze the speed requirement of the FBMDs. The required degree of FBMD controllability determines the level of performance demanded from the controller, as shown in Sections 3.4 and 3.5. The operating frequency is based on the frequency response of the FBMDs and the desired level of controllability. Section 3.6 describes the speed requirement of the design. Section 3.7 discusses the remaining design constraints, size and power.

3.2 Theoretical Flexure Beam Mirror Device Operating Frequency Range

The frequency response of the flexure beam mirror device (FBMD) above the resonant frequency determines the minimum design frequency of the controller. The resonant frequency predicted in Equation (2-14) contains two variables, the mass of the mirror M and spring constant k. However, since both variables are mirror dependent, the resonant frequency becomes a range of frequencies if more than one mirror design is to be modulated. In order to estimate the range of frequencies, six different mirror devices, with varying flexure width and mirror sizes, were fabricated and investigated.

Neglecting the topology of the mirror devices simplifies the analysis of the mirror mass. Multiplying the area of the mirror per layer by the thickness of the layer yields the volume of the mirror contributed by each layer. The mass of each layer is then calculated by the product of the calculated volume and density of each layer. The summing of all the masses of each layer yields the total mass. Table 3-1 lists the material parameters for each fabrication layer of the FBMD's design. Figure 3-1 shows the Poly1 layer with the mirror area and its associated dimensions highlighted.

Table 3-1. MUMPS Fabrication Layer Material Parameters [8,13].

Layer	Density (kg/m^3)	Thickness
Poly1	2330	2 μm
Oxide2	2330	1.5 μm
Poly2	2330	750 nm
Metal (Gold)	19300	500 nm

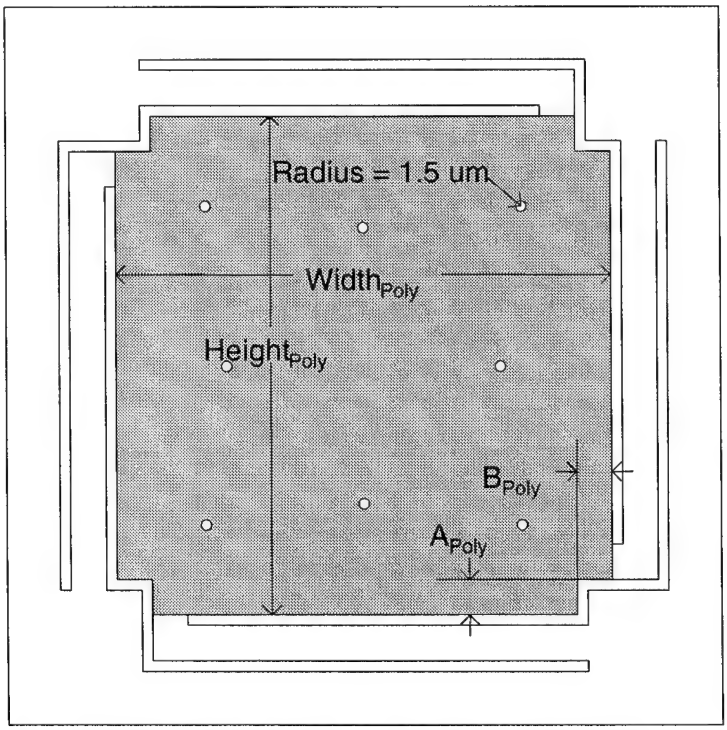

Figure 3-1. Poly1 Mirror Dimension Definition Schematic.

Table 3-2 details the Poly1 dimensions of each mirror and the mass of the mirror due to the Poly1 layer. The shape and dimensions shown in Figure 3-1 also apply for layer Poly2. Table 3-3 itemizes the Poly2 dimensions in Figure 3-1 for each mirror and the calculated masses.

Table 3-2. Poly1 Masses of Frequency Test Mirrors.

Flexure Width	$Width_{Poly1}$	$Height_{Poly1}$	A_{Poly1}	B_{Poly1}	$Mass_{Poly1}$ (grams)
5 μm	151 μm	151 μm	15 μm	15 μm	$98x10^{-9}$
6 μm	149 μm	149 μm	14 μm	14 μm	$96x10^{-9}$
7 μm	147 μm	147 μm	13 μm	13 μm	$94x10^{-9}$
8 μm	145 μm	145 μm	12 μm	12 μm	$92x10^{-9}$
9 μm	143 μm	143 μm	11 μm	11 μm	$90x10^{-9}$
10 μm	141 μm	141 μm	10 μm	10 μm	$88x10^{-9}$

Table 3-3. Poly2 Masses of Frequency Test Mirrors.

Flexure Width	$Width_{Poly2}$	$Height_{Poly2}$	A_{Poly2}	B_{Poly2}	$Mass_{Poly2}$ (grams)
5 μm	148 μm	148 μm	15 μm	15 μm	$73x10^{-9}$
6 μm	146 μm	146 μm	14 μm	14 μm	$72x10^{-9}$
7 μm	144 μm	144 μm	13 μm	13 μm	$70x10^{-9}$
8 μm	142 μm	142 μm	12 μm	12 μm	$68x10^{-9}$
9 μm	140 μm	140 μm	11 μm	11 μm	$67x10^{-9}$
10 μm	138 μm	138 μm	10 μm	10 μm	$65x10^{-9}$

Figure 3-2 describes the Oxide2 schematic with the "trapped oxide" highlighted. All the frequency test mirrors have the same dimensions. Using the dimensions from Figure 3-2 and the material parameters from Table 3-1, the "trapped oxide" contribution to the mass of the mirror is $7x10^{-9}$ grams.

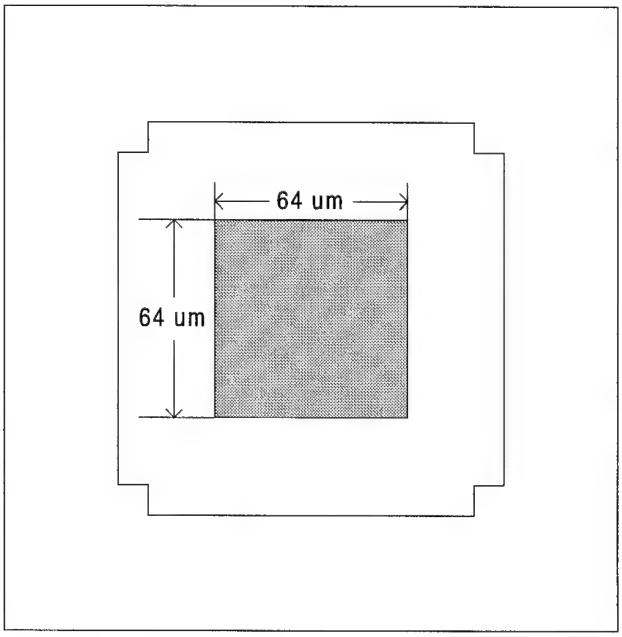

Figure 3-2. Oxide2 Mirror Dimension Definition Schematic.

Figure 3-3 defines the size and shape of the Metal layer. Using Figure 3-3 and Table 3-1, the mass of the mirror added by the Metal layer is 27×10^{-9} grams.

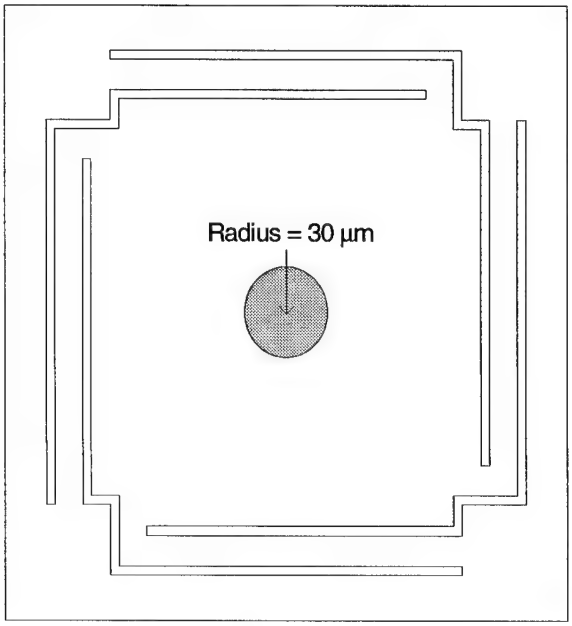

Figure 3-3. Metal Mirror Dimension Definition Schematic.

Summing the masses of Poly1 from Table 3-2, Poly2 from Table 3-3, the "trapped oxide", and Metal yields the total mirror mass. Table 3-4 summarizes the total mirror mass as previously described and flexure mass for each test device using the geometry from Figure 3-4 and the material parameters from Table 3-1. Since the masses of the mirrors are over an order of magnitude greater than the masses of the flexures, the masses of the flexures are neglected from the frequency response calculations.

Table 3-4. Mass Summary of Frequency Test Mirrors.

Flexure Width	Flexure Mass (grams)	Mirror Mass (grams)
5 μm	10×10^{-9}	206×10^{-9}
6 μm	12×10^{-9}	202×10^{-9}
7 μm	14×10^{-9}	198×10^{-9}
8 μm	16×10^{-9}	194×10^{-9}
9 μm	19×10^{-9}	190×10^{-9}
10 μm	21×10^{-9}	187×10^{-9}

The geometries of the flexures and the mechanical properties of the flexure material determine the spring constant, based upon Equation (2-3). Figure 3-4 details the length of the flexures and the width definition of flexures. As shown in Table 3-2 through Table 3-4, the flexure width varies from 5 μm to 10 μm.

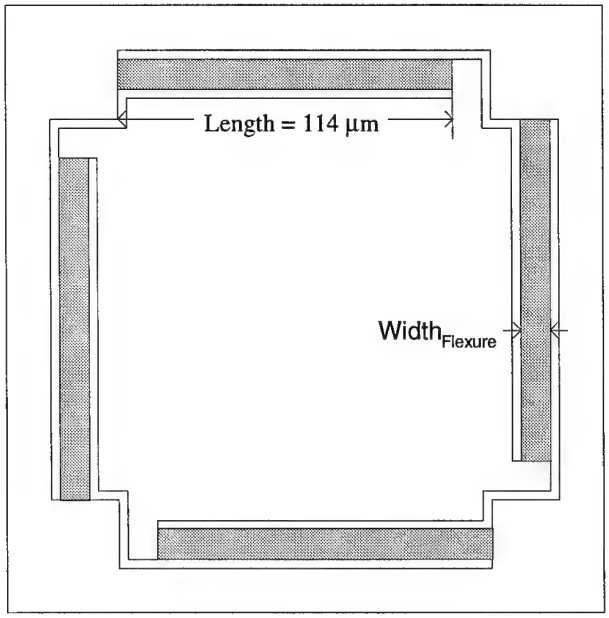

Figure 3-4. Poly1 Flexure Dimension Definition Schematic.

Using the total mass from Table 3-4, the mechanical properties of the Poly1 layer from Table 3-5, and the geometries shown in Figure 3-4, the theoretical resonant frequency of each mirror is calculated in Table 3-6.

Table 3-5. Poly1 Material Mechanical Properties [13, 14].

Modulus of Elasticity (E)	Residual Material Stress (σ)	Poisson's Ratio (υ)
160 GPa	9.0 MPa (Compressive)	0.22

Table 3-6. Theoretical Resonant Frequencies of Four Flexure Poly1 FBMDs.

Flexure Width	Resonant Frequency (kHz)
5 µm	44
6 µm	49
7 µm	53
8 µm	58
9 µm	61
10 µm	65

Based on Table 3-6, the theoretical resonant frequencies of all six FBMDs range from approximately 44 kHz to 65 kHz. Figure 2-15 shows that the response of the FBMD should diminish as the frequency increases above resonance. At and above some frequency, defined as the cut-off frequency, the position response of the mirror will be negligible. This cut-off frequency must be found via experimental measurements, as described in Section 3.3.

3.3 Frequency Response Verification

In addition to predicting the resonant frequency, Equation (2-13) shows that the frequency response of the mirror continued to diminish at frequencies above the resonant frequency. The frequency response for all six mirrors described in the previous section was experimentally observed. Figure 3-5 depicts the experimental setup of the frequency response test fixture. This test fixture operates as a Michelson interferometer. A laser beam splits into a reference beam and an incident beam. The incident beam travels through the microscope and onto the FBMD under test. The FBMD reflects the incident beam back to the beam detector. At the detector, the reflected beam interferes with the reference beam. The difference in phase between the reflected and reference beams determine the intensity at the detector. As the FBMD deflects, the phase difference varies and the intensity at the deflector changes. Thus, the intensity at the detector is proportional to the deflection of the FBMD [2].

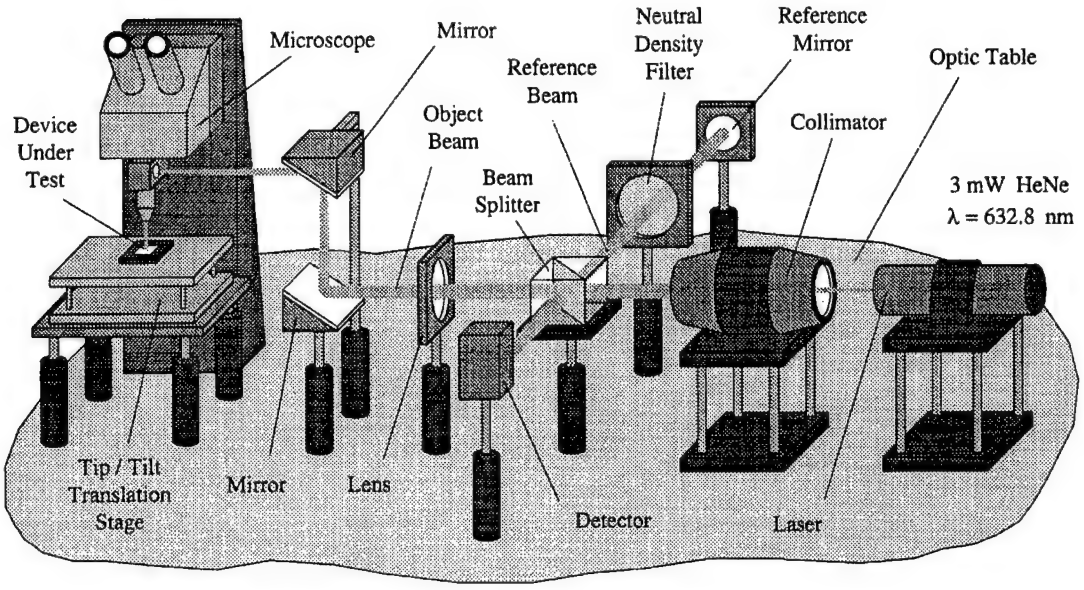

Figure 3-5. Experimental FBMD Frequency Response Test Fixture [2].

A sinusoidal voltage applied to the FBMD produces a frequency response that can be observed as intensity variations of the light at the detector. However, precise measurements are difficult to obtain due to high noise levels caused by external vibrations. The optical table reduces the amplitude of most external vibrations, but many vibrations in the test fixture are transmitted to the detector. In addition, the output of the detector is proportional to a change in position of the FBMD, not the actual position of the FBMD. Complex mathematical post-measurement computations are needed to extract the position of the FBMD as a function of the applied voltage. Fortunately, the absolute position measurement of the FBMD is not necessary. Only the detection of a response is needed. By observing the near-static response of the FBMD using an oscilloscope displaying the output of the detector, the oscilloscope was set to detect any

output from the detector that was greater than approximately one percent of the near-static response. Using a sweeping function generator, a linear sweep of the frequencies at and above the theoretical frequency of the 7 μm flexure width FBMD was performed. The response decreased as the frequency was increased above the calculated resonant frequency, but was observable up to 67 kHz, which was labeled the cut-off frequency. No response was detected between 67 kHz to 5 MHz, which was the frequency limit of the detector. The remaining five mirror devices were observed to have similar responses. However, the frequency response investigation of the remaining five mirrors was limited to below 250 kHz. The greatest cut-off frequency was approximately 80 kHz for the 10 μm flexure width FBMD. All observations were made with the mirrors in a vacuum of at least 20 mTorr to limit the squeeze film damping effect[2] [6]. In a laboratory environment of approximately 1 Torr, the frequency response of the mirrors decreases by at least a factor of four.

3.4 Mirror Position Resolution

The pulse width modulation theory explained in Section 2.6 presents the duty cycle as a continuously variable analog function. However, in digital designs, this analog function must be transformed into discrete values. The discrete values are produced by quantitizing the analog value into 2^X discrete ranges, where X is the number of bits in the

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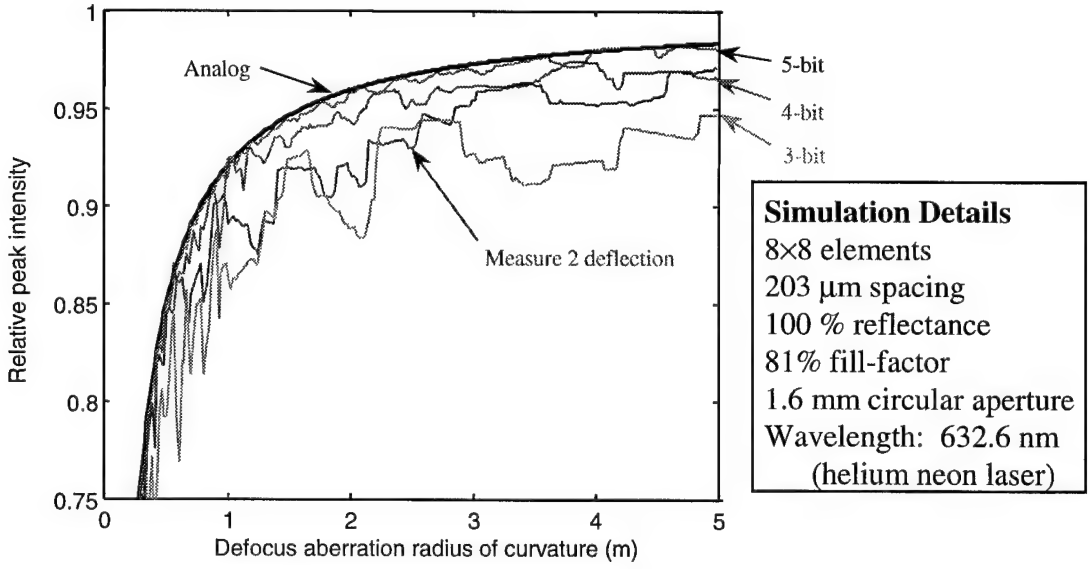
[2] Squeeze film damping – effect in which gases are analyzed as a viscous fluid which affects the frequency response of the device [15].

digital value. Previous research shows that the optical performance as a function of the mirror position resolution approximates the analog response for 3-bit resolution or greater [6]. Figure 3-6 presents an example of the optical performance of a mirror for several given resolutions. The ability of the mirror array to correct an aberration is limited by the resolution of the mirror elements and the radius of curvature of the aberration relative to the size of the mirror elements. The degree of correction is proportional to the relative peak intensity. If the mirror can be positioned only at discrete deflections, the optical performance decreases. However, as shown in Figure 3-6, as the number of discrete positions increases, the optical performance of the mirror array approaches the best-case scenario of an analog value.



Modulo $\lambda/2$ deflection yields $\lambda/(2x2^N)$ deflection resolution for N-bits
(i.e. $\lambda/16$ for 3-bits, $\lambda/32$ for 4-bits, $\lambda/64$ for 5-bits)

Figure 3-6. Example Optical Response as a Function of Resolution [6].

3.5 Performance

The performance of the controller is determined by its ability to accurately position the mirror. This positioning is determined by the data word size. Figure 3-6 shows that any word size 5-bits or greater produces a good approximation of the analog value. However, as the word size is increased, the approximation improves. An 8-bit standard data word choice provides excellent controller performance and increases compatibility with conventional microprocessors.

3.6 Speed

Sections 3.2 and 3.3 demonstrate that the mirrors cannot significantly respond to any frequencies above approximately 80 kHz. Rounding this value up to 100 kHz creates a margin of safety and allows for an increase in the range of designs that can be modulated without modification to the controller. With 256 equally-spaced discrete ranges resulting from the 8-bit data word size, the controller's operating frequency is 25.6 MHz. The speed and performance are the major design considerations and will not be compromised.

3.7 Size and Power Consumption

Size and power consumption are the other major design consideration for a VLSI project. Size is generally inversely proportional to the speed. The design will be made as small as possible while maintaining the 25.6 MHz design frequency. Since the design is comprised of standard cells, the transistor size is not changeable. A reduction of the gate

count and its associated routing is the primary method to reduce the size of the design. Reducing the gate count also minimizes the power consumption.

3.8 Summary

The FBMD frequency response theory predicts the greatest response frequency of the mirror. The analysis in Section 3.2 calculates the theoretical resonant frequency for each of the six test FBMDs. Section 3.3 describes the experiment used to verify the resonant frequency of each FBMD. In addition, Section 3.3 verifies that the FBMDs will not respond to any frequencies above the cut-off frequency. Section 3.4 shows that quantitizations at and above 3 bits adequately approximate the analog FBMD response [6]. Section 3.5 describes the choice of an 8-bit word size based upon the mirror analysis presented in Section 3.4. Given the 8-bit word size choice and frequency response of the FBMDs, Section 3.6 determines that the design's operating frequency should be 25.6 MHz. Size and power consumption are to be minimized given the above design constraints, as stated in Section 3.7.

Based upon the above analysis and design considerations, a controller implementing these choices should be able to control the deflection of the FBMDs. Chapter 4 covers the implementation of such a controller.

4 Gate-level Design and Implementation of the Mirror Controller

4.1 Introduction

The pulse width modulation controller implements the high-level decisions discussed in Chapter 3. It is realized using a very large scale integration (VLSI) design. The specific fabrication process imposes several design constraints, as described in Section 4.2. The top-level input/output is specified in Section 4.3. In addition, the system is divided into functional blocks in Section 4.3. Sections 4.4 through 4.7 detail the functional blocks developed in Section 4.3. Section 4.8 describes additional features added to ease testing.

4.2 Design Constraints

The pulse width modulation controller is fabricated using the MOSIS foundry services, specifically the AMI 1.2 μm process in a TinyChip design. The TinyChip is 2.20 x 2.20 mm die packaged in a 40-pin chip carrier. The input/output (I/O) pads and power pads were supplied by MOSIS in a standard pad-frame designed to fit the 40-pin chip carrier. The TinyChip implementation is a good choice for prototyping due to a 10 week fabrication time and the relatively low cost [16].

The digital interface to the design should conform to a standard bus consisting of DATA, ADDRESS, and STROBE signals. The 8-bit data word size defined in Section 3.5 requires 8 DATA pins of the 40 pin package. The number of address lines is a function of the number of output channels such that the number of output channels is less

less than or equal to 2^N, where N is the number of address lines. The STROBE signal marks the stability of the DATA signals and prompts the controller to store the information on the DATA bus. The choice of sixteen OUTPUT channels defines at least four address lines. Subtracting one CLOCK signal and four power pins leaves six pins unassigned, of which two are used as CONTROL signals and the other four are applied to the ADDRESS bus. Figure 4-1 illustrates the port assignments without power pins.

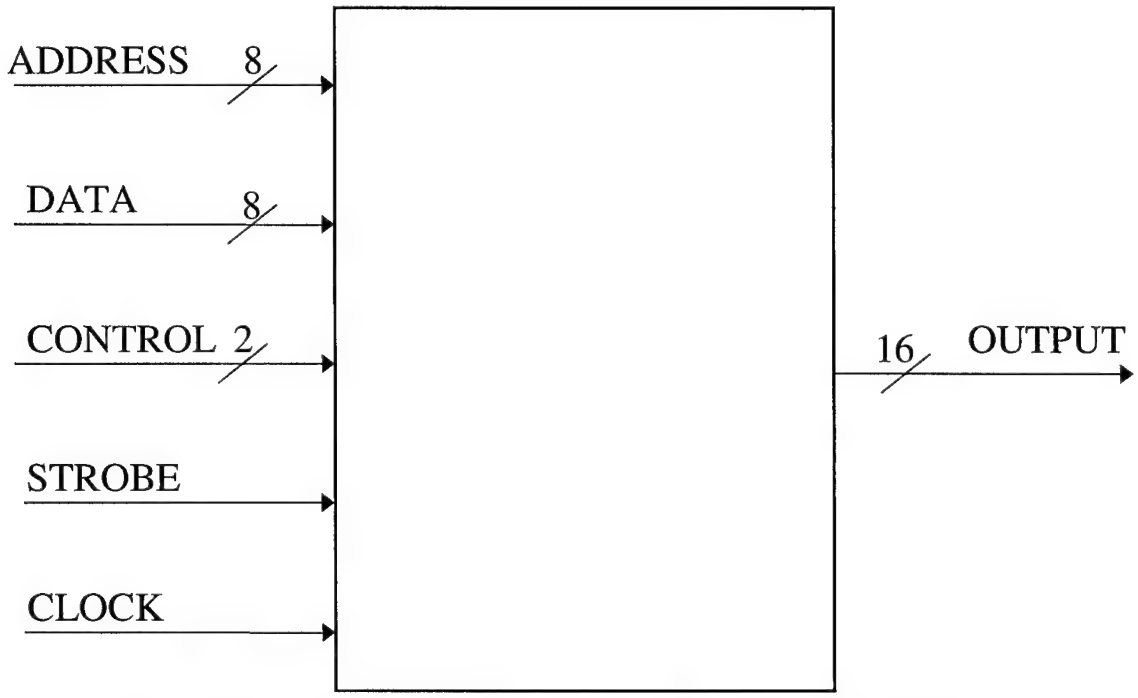


Figure 4-1. Port Assignment of Pulse Width Modulation Controller.

4.3 Design Overview

The design approach chosen employs a top-down[3] design approach to the implementation of the pulse width modulator. Starting with the port assignment shown in Figure 4-1, the system will be logically divided into functional blocks, as shown in Figure 4-2.

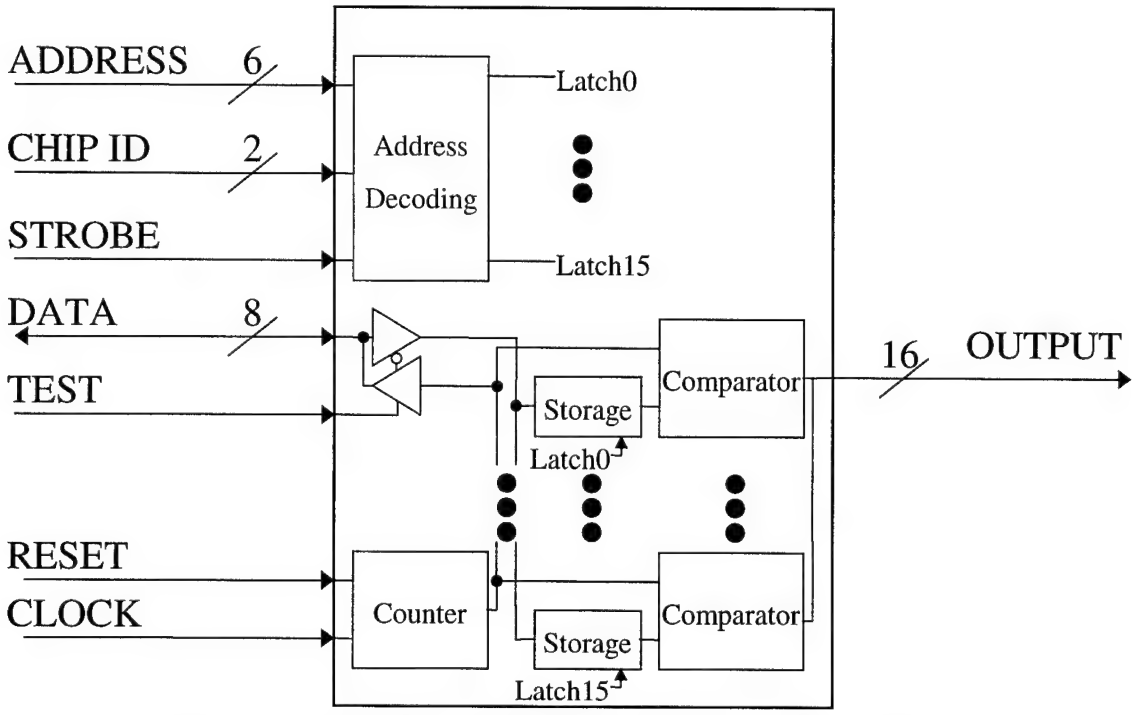


Figure 4-2. Pulse Width Modulation Controller Block Diagram.

The 100 kHz update frequency chosen in Section 3.6 must be divided into 256 equal-time intervals of approximately 70 ns each. Rather than attempting to divide a 100 kHz clock into 256 equally-spaced intervals, a 25.6 MHz clock defines the 70 ns interval

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[3] Top-down design – design methodology in which the complete system is viewed as a whole and then divided into various blocks which perform specific subsets of the total functionality [17].

and is applied to the CLOCK pin. Thus, 256 CLOCK pulses, or intervals, define one update period. However, using this method, the intervals must be indexed in order to determine the specific number of intervals that have expired. This analysis suggests that an accumulator should be used. The 8-bit data word size chosen in Section 3.5 leads to in an 8-bit accumulator named COUNTER.

The output of the COUNTER, denoted as COUNT, is provided to each of the OUTPUT channels. Each individual output channel must individually determine whether the prescribed number of CLOCK cycles, defined by COUNT, have expired. A COMPARATOR for each output channel continuously monitors COUNT (see Figure 4-2). The COMPARATOR performs an unsigned 8-bit magnitude comparison between COUNT and the user-specified duty cycle value. Because COUNT is an unsigned binary number which ranges from 0 to 255, COUNT will transition from 255 to zero on the 256^{th} CLOCK pulse. This rollover automatically forces each COMPARATOR to assert its OUTPUT and defines the update period.

The prescribed number of CLOCK cycles, defined as duty cycle value, is a variable written by the user to each OUTPUT channel (see Figure 4-2) using the DATA bus, ADDRESS bus, and STROBE signal. The four least significant bits of the ADDRESS bus define where the information on the DATA bus is written. However, four extra ADDRESS signals were defined in Section 4.2. These signals are defined as the most significant two bits of the ADDRESS bus and two CHIP SELECT signals (see Figure 4-2). The ADDRESS DECODER logic is enabled only when the CHIP SELECT signals equal the two most significant bits of the ADDRESS bus. By providing four controllers with mutually exclusive CHIP SELECT values, the remaining inputs for the

four controllers can be connected in parallel without any additional decoding logic. A schematic showing this type of connection is shown in Appendix D. When the controller is selected, the ADDRESS DECODER uses the four least significant bits of the ADDRESS bus and the STROBE line to create sixteen channel LATCH signals (see Figure 4-2).

The controller must have a mechanism to store the duty cycle value for each OUTPUT channel since the information is only present at the DATA bus for a short period of time. Each channel will have a STORAGE block that will capture the information on the DATA bus when its associated LATCH signal is asserted (see Figure 4-2).

The remaining two CONTROL inputs are used for design-for-testability features. A signal RESET asynchronously resets the CLOCK. The other signal, TEST, determines the direction of the DATA bus. When the DATA bus is an output, COUNT is written (see Figure 4-2).

4.4 Counter

The COUNTER is a Moore-type[4] finite state machine. The next value of the COUNT is calculated by adding one to the current COUNT. At the clock edge, the next value is loaded into the state registers, and the process repeats. An exception to the

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[4] Moore machine – a finite state machine in which all the outputs change only on or during the clock edge [17].

incremental counting occurs when the RESET signal is asserted causing the output of all the registers to clear asynchronously.

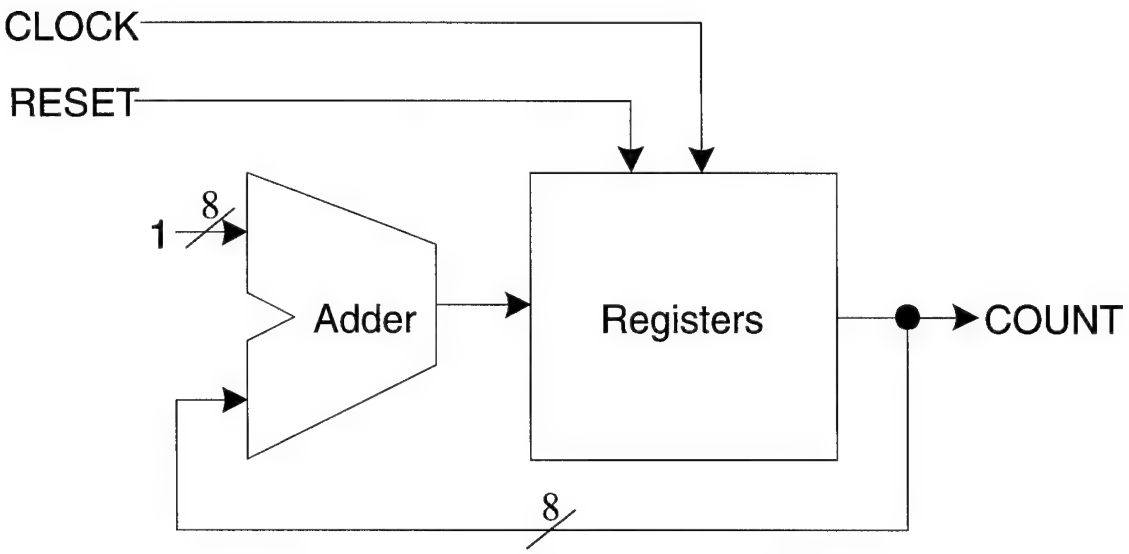

Figure 4-3. Block Diagram of the Counter.

The adder shown in Figure 4-3 increments the current COUNT by one. Several adder architectures were investigated, specifically ripple-carry[5], carry-lookahead[6], and carry-select[7] adders. The 25.6 MHz design frequency eliminated the ripple-carry adder due to the propagation delays. The relatively large gate count of the carry-select adder prohibited its implementation. However, the carry-lookahead adder consumes the

---

[5] Ripple-carry adder – adder in which two numbers are added one bit at a time with the carry input of each bit resulting from the carry output of the previous bit [17].

[6] Carry-lookahead adder – adder in which the output is determined exclusively by the carry propagate and generate signals and the primary inputs using combinational logic [17].

smallest physical floorspace of the investigated designs capable of operating at the 25.6 MHz design frequency. Equation (4-1) describes the combinational carry-lookahead logic necessary to generate the carry input at each stage [17].

$$C_i = \sum G_i + P_i \bullet C_{i-1} \tag{4-1}$$

where G_i is the carry generate and P_i is the propagate signal as defined by [17]:

$$G_i = A_i \bullet B_i$$
$$P_i = A_i + B_i$$

However, the design of the carry-lookahead adder reduces to a sequence of half-adders[8] and the associated carry-lookahead logic due to the addition of the constant one to the current count. Expanding Equation (4-1) and setting the B input equal to the constant one reduces to Equation (4-2).

$$C_i = Count_i \oplus \left(Count_{i-1} \bullet Count_{i-2} \bullet \ldots \bullet Count_0\right) \tag{4-2}$$

The registers are implemented as eight one-bit registers with an active-low asynchronous RESET and a falling-edge CLOCK. Figure 4-4 shows the schematic of the counter with Boolean optimization applied to minimize the physical floorspace of the design.

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[7] Carry-select adder – adder in which both the result is calculated for both the carry input conditions and the output is selected based upon the actual carry input [17].

[8] Half-adder – adder with only two inputs as opposed to a full-adder with two inputs and a carry input [17].

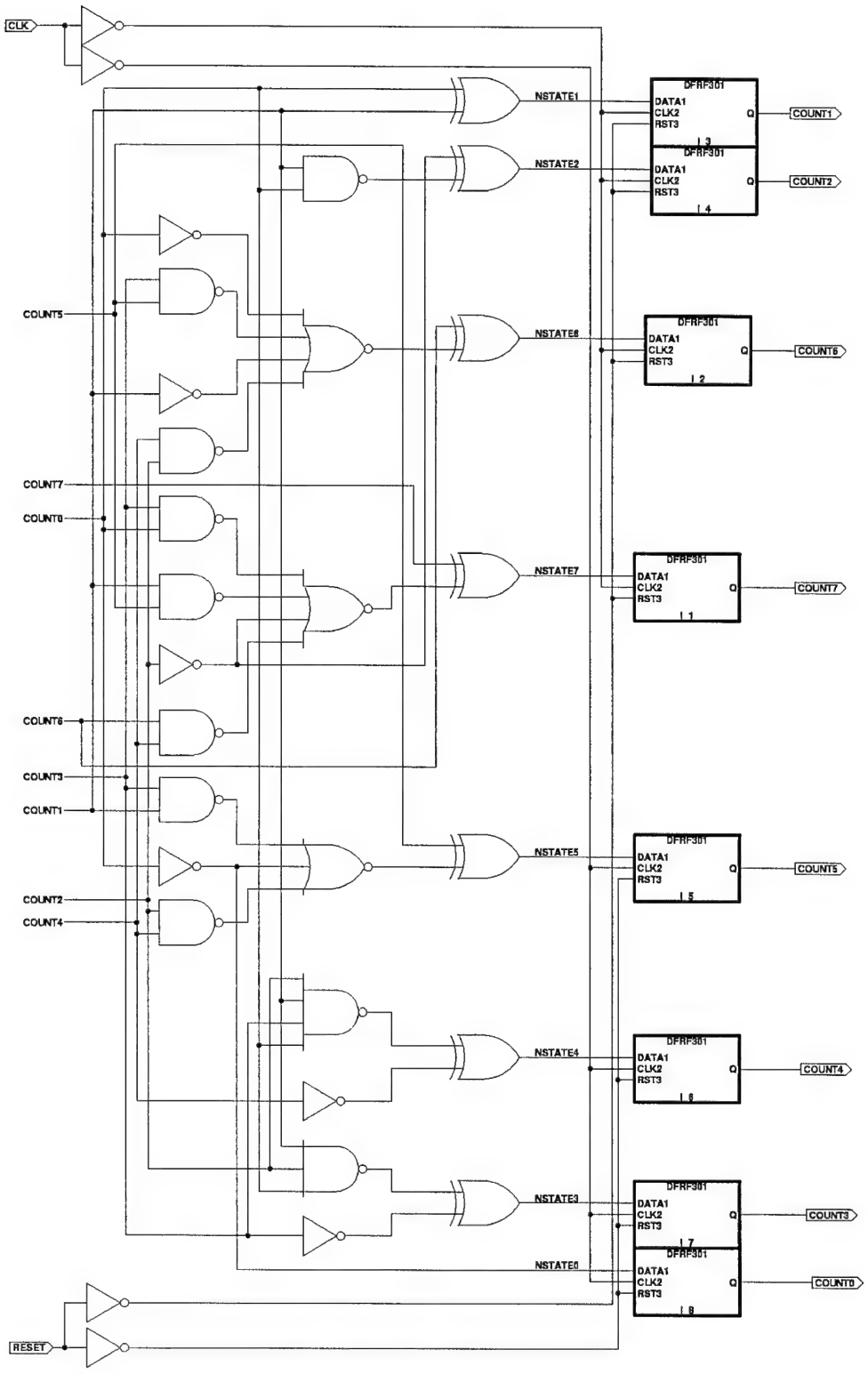

Figure 4-4. Counter Schematic.

4.5 Comparator

The combinational logic that performs the less-than unsigned magnitude comparison implements the COMPARATOR. The OUTPUT of the COMPARATOR is only high when the current COUNT from the COUNTER is less-than the duty cycle value. Figure 4-5 provides the gate-level schematic for the COMPARATOR. Each OUTPUT channel requires one COMPARATOR.

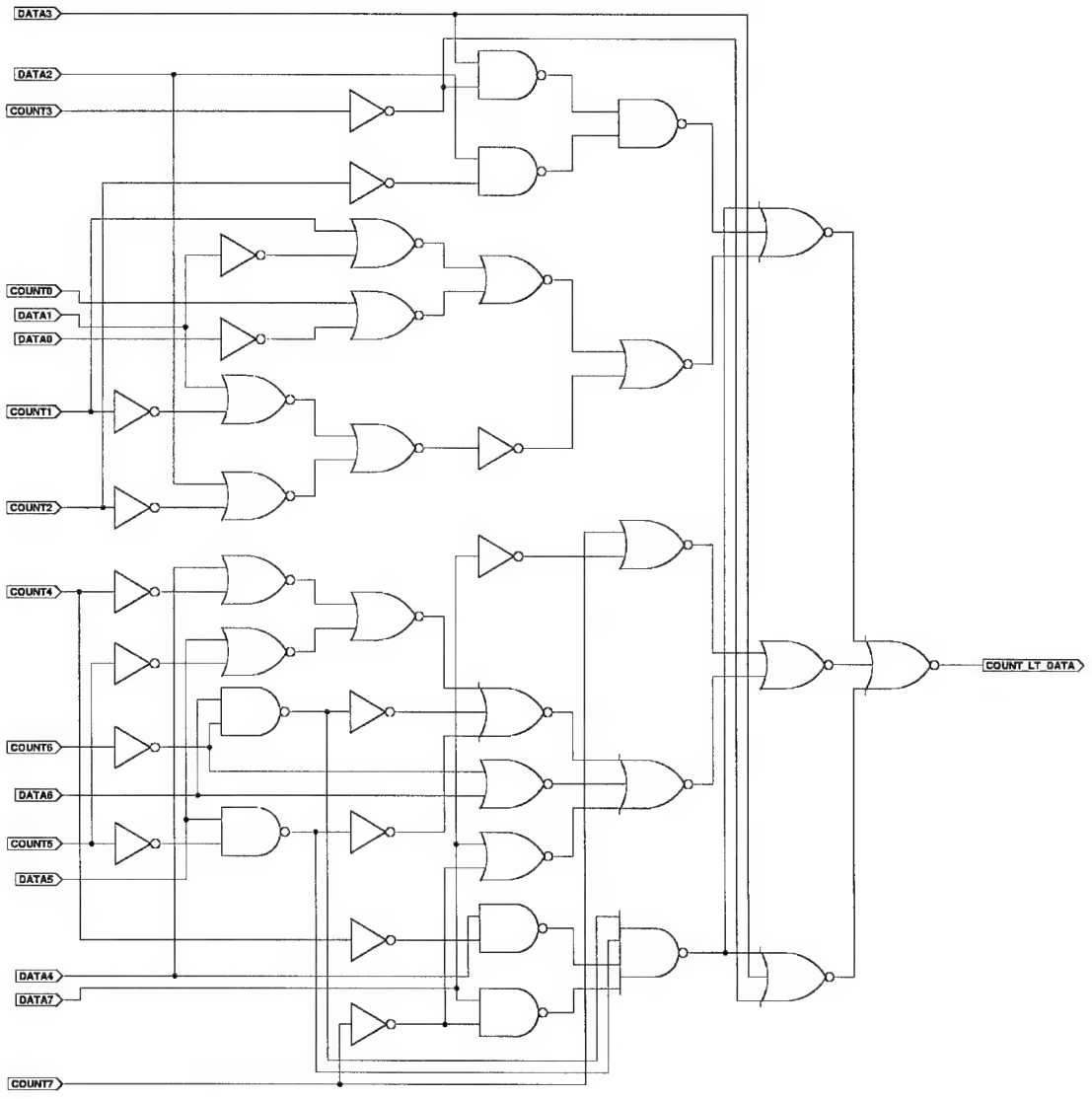

Figure 4-5. Less-Than Comparator Schematic.

4.6 Storage Latches

Eight one-bit latches retain the last value written to them by capturing the information from the DATA bus when the active-low LATCH inputs are asserted. Two inverters are used to reduce the fanout and invert the polarity of the LATCH signals as evident in Figure 4-6. Each OUTPUT channel requires one eight-bit STORAGE latch.

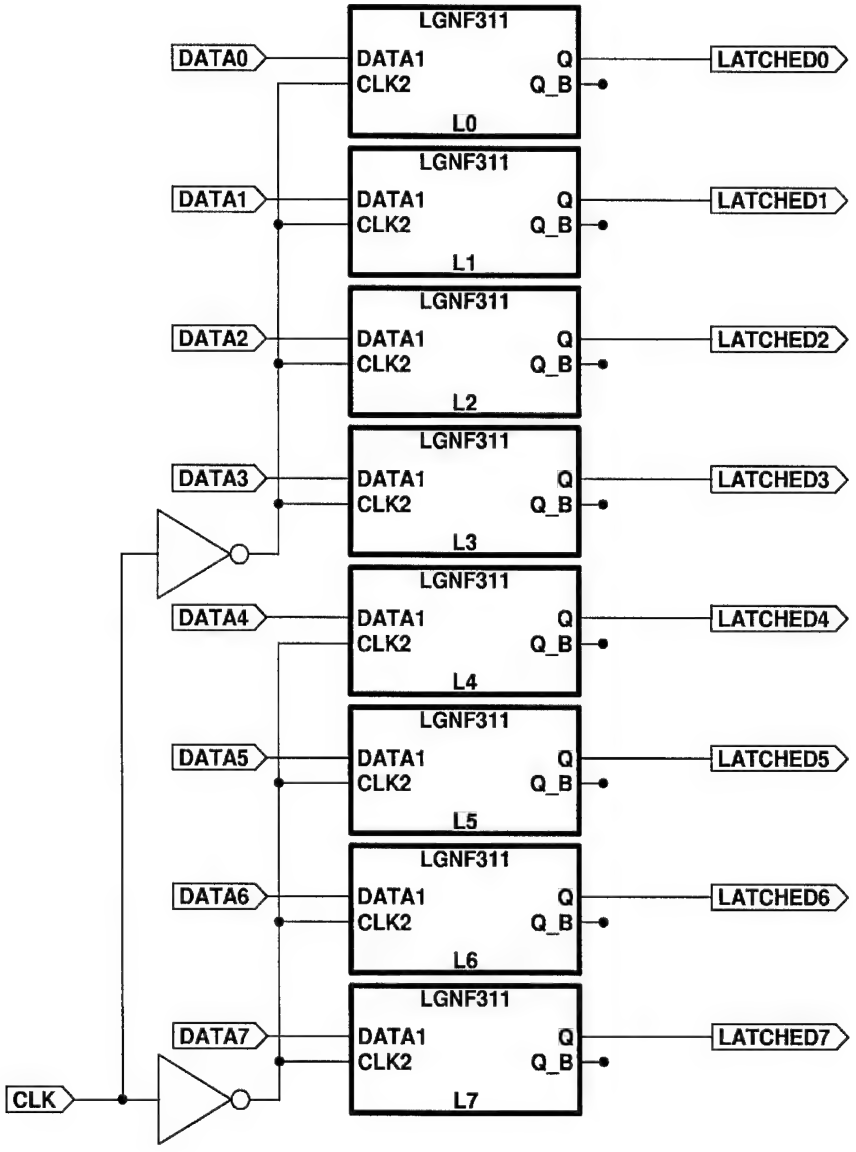

Figure 4-6. Eight-Bit Storage Latch Schematic.

4.7 Address Decoder

ADDRESS DECODING logic specifies which channel's STORAGE latch receives the information on the DATA bus. The upper two significant bits of the ADDRESS bus are compared to the CHIP ID bus. If equal, the ADDRESS DECODING logic performs a four-to-sixteen demultiplex function. Else, the outputs remain unasserted. The STROBE input gates the four-to-sixteen address demultiplex function producing sixteen mutually exclusive LATCH signals, as shown in Figure 4-7.

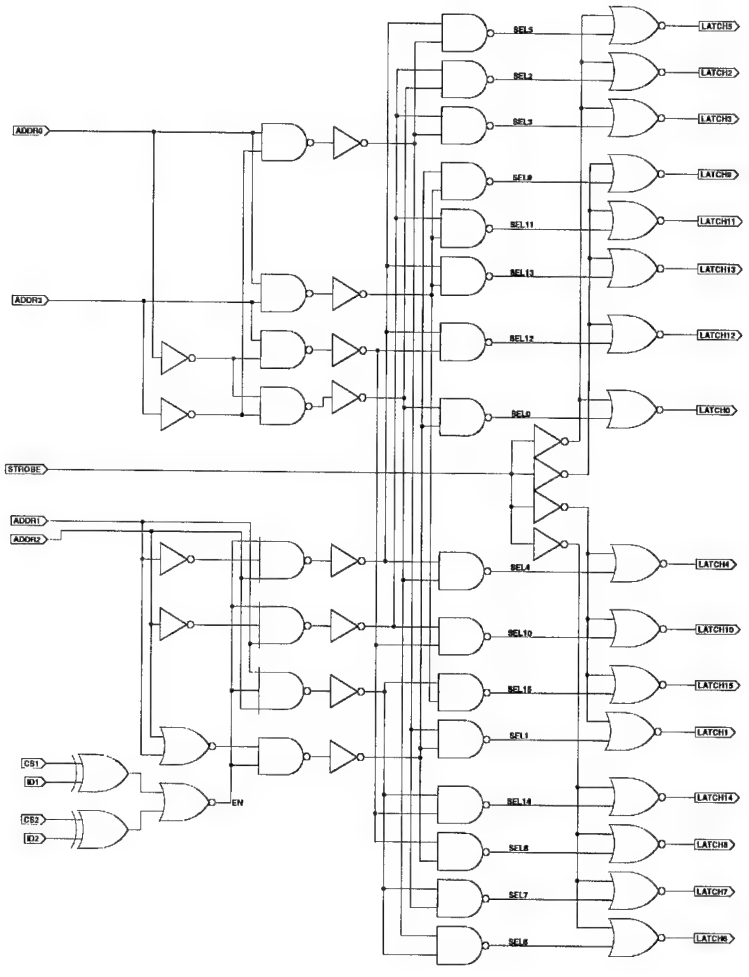

Figure 4-7. Address Decoding Schematic.

4.8 Design for Testability

Design for testability (DFT) consists of three aspects: controllability, observability, and predictability. Controllability defines the ability to directly control the stimuli at the input nodes of the circuit under test. Observability is the ability to investigate the value present at the output nodes of the circuit under test. Predictability refers to the ability to know the output of a circuit, given a known set of inputs. Incorporating DFT features into a design simplifies testing and verification [18].

Two signals, RESET and TEST, allow sufficient control and observability of the circuit operation. The TEST line allows the observation of COUNT. Observing COUNT verifies the correct operation of the COUNTER and enables further testing of the remaining circuitry. The RESET signal asynchronously changes the current COUNT to zero. Using a combination of the CLOCK and RESET signals, COUNT can be directly controlled. By directly controlling COUNT, the correct operation of the COMPARATORS, STORAGE latches, and ADDRESS DECODING can be verified by observing the OUTPUT signals. However, no information about the internal values of the LATCH signals, STORAGE latches, or COMPARATOR is observable. Without the ability to observe the internal values of these nodes, it may not be possible to determine the faulty functional block should a fault occur.

4.9 Design Methodology and Tools

Each functional block described previously was synthesized from VHSIC[9] hardware description language (VHDL) using the Synopsys Design Analyzer (DA) [19], Synopsys Graphical Editor (SGE) [20], and the Octtools [21]. The DA, SGE and Octtools are compatible with and configured for the Lager standard cell library [21], which was used to implement the gates shown in the previous schematics. However, the Octtools were not able to compactly place-and-route the entire design. The interconnectivity of the functional blocks and the connectivity of the core logic to the MOSIS-supplied pad frame [16] were manually routed using Magic [21]. The core logic was simulated using IRSIM [21] and HSPICE [22] to verify functionality and estimate timing and power consumption.

4.10 Summary

The implementation of the controller is simplified by investigating the interface to-and-from the design and by breaking the functionality of the system into several smaller functional blocks. The design considerations that determine the controller's port definition are discussed in Section 4.2. The system is partitioned into functional blocks, which are described in Section 4.3. These functional blocks are discussed down to the gate level implementation in Sections 4.4 through 4.7. The design-for-testability features included in the controller and the approach to verification of the controller design are

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[9] VHSIC- very high speed integrated circuit

detailed in Section 4.8. The methodology and design tools used to implement the pulse width modulation controller are described in Section 4.9. The experiments necessary to verify the controller and validate the ability of the controller to modulate the deflections of the flexure beam mirror devices are described in Chapter 5.

5 Experimental Setup and Procedures

5.1 Introduction

The implementation of the controller discussed in Chapter 4 must be verified after fabrication. The "as-fabricated" investigation verifies the correct operation of the controller design or detects problem area(s) in the design and/or fabrication. The controller design verification experiments are described in Section 5.2.

The ability of the design to correctly control the deflection of the flexure beam mirror device (FBMD) also needs to be demonstrated. Additionally, a baseline measurement must be made to evaluate the performance of the controller. The experiments that measure both the baseline and controller deflection are explained in Section 5.3.

5.2 VLSI Pulse Width Modulation Design Verification

Visual inspection and preliminary conductivity checks increase the level of confidence in the correct design and fabrication of the pulse width modulation design, named PWM16. In addition, the visual inspection and preliminary conductivity checks, described in Section 5.2.1, provide a sanity check for design verification.

The operation of the PWM16 is investigated after the visual inspection and conductivity measures are successfully performed. The design-for-testability features described in Section 4.8 enable the testing of individual portions of the design separately to reduce the effort necessary to validate proper operation. Figure 4-2 shows the

functional blocks of the PWM16. Section 5.2.2 includes the tests necessary to validate the functional block COUNT. The remaining portion of the design, namely the ADDRESS DECODING and the sixteen sets of STORAGE latches and COMPARATORs can be tested if the COUNT is known. The test that verifies proper operation of the OUTPUTs is presented in Section 5.2.3.

5.2.1 PWM16 Fabrication Inspection

Both a visual inspection and an electrical resistivity test can detect catastrophic errors in the design and fabrication sequence. First, a visual inspection under a microscope ensures the correct orientation of the design wafer inside the chip carrier. In addition, the visual inspection is used to detect missing connections or faulty bonding to the design wafer or the chip carrier, as well as any foreign material on the wafer surface. Next, the bonding of the design wafer to the chip carrier and the pad-to-pin signal paths are visually inspected to validate the bonding diagram. Finally, resistivity measurements between all power and ground supply pins are performed.

5.2.2 PWM16 COUNT Verification Experiment

The COUNT signal verification experiment confirms the proper operation of the COUNT portion of the design once the visual inspection and conductivity checks have been successfully accomplished. Using the direct controllability of the COUNT signals with the RESET and CLOCK pins and the direct observability via the TEST and DATA pins as shown in Figure 4-2, the HP82000 IC Evaluation System [23] stimulates and monitors the signals of the PWM16.

The sequence of test events that the HP82000 performs is as follows:

1. Define all pin configurations, timings, and voltage levels in the HP82000 software
2. Insert PWM16 into HP82000
3. Assert TEST to observe COUNT via the DATA port
4. Set COUNT to zero by asserting RESET
5. Deassert RESET
6. Monitor COUNT on DATA signals and verify COUNT equals zero
7. Apply CLOCK pulse
8. Verify COUNT is incremented by one.
9. If COUNT is not equal to 255, goto step 7
10. Apply CLOCK pulse
11. Verify COUNT equals zero

5.2.3 PWM16 OUPUT Verification

The remaining portions of the design can be confirmed by observing each of the signals present at the output pins while stimulating the input pins once the COUNT portion of the PWM16 is verified. These observations are made most easily with an oscilloscope connected to an individual output channel. The control of the input pins is provided by a PC-compatible computer. Appendix D shows the schematic for controlling up to four PWM16 chips simultaneously. The logic shown in the schematic memory-maps all four PWM16s into the address space of the computer at the base address specified by the address switches SW1 and SW2. Appendix E contains the software used to control the design. The software performs the following tasks:

1. Turn off all OUTPUTs
2. Set OUTPUT channel pointer to the first OUTPUT channel
3. Increment value at OUTPUT channel pointer
4. Print the number of the OUTPUT channel pointer and duty cycle value
5. Wait for user to press any key
6. If value at OUTPUT channel pointer is not equal to zero, goto step 3
7. If OUTPUT channel pointer is not pointing to the last OUTPUT channel, increment OUTPUT channel pointer and goto step 3
8. Exit program

The duty cycle of an individual channel is observed after sequencing through step 4 during every iteration. In addition, the OUTPUT of all other channels is periodically verified after step 4. All OUTPUTs not currently under control should be a constant logic low.

5.3 FBMD Measurement Experiment

The baseline deflection of an FBMD as a function of the controlling input is measured using a Zygo Maxim 3-D [24], an oscilloscope, a power supply and the PWM16 ISA card following the PWM16 verification experiments of Section 5.2. The Zygo is a commercial microscope interferometer that can make relative vertical height measurements in the nanometer range [24]. By creating a height profile of the flexure, the deflection can be computed as the difference in height between the fixed end of the flexure and the end connected to the mirror. The height profile is created by graphically selection one point at each end of the FBMD's flexure and creating a cross-sectional height contour. Figure 5-1 presents the FBMD and illustrates the scan path along which the height contour is created. The Zygo displays the maximum difference in height between the floating and anchored points along the scan path. This maximum difference in height is recorded as the deflection.

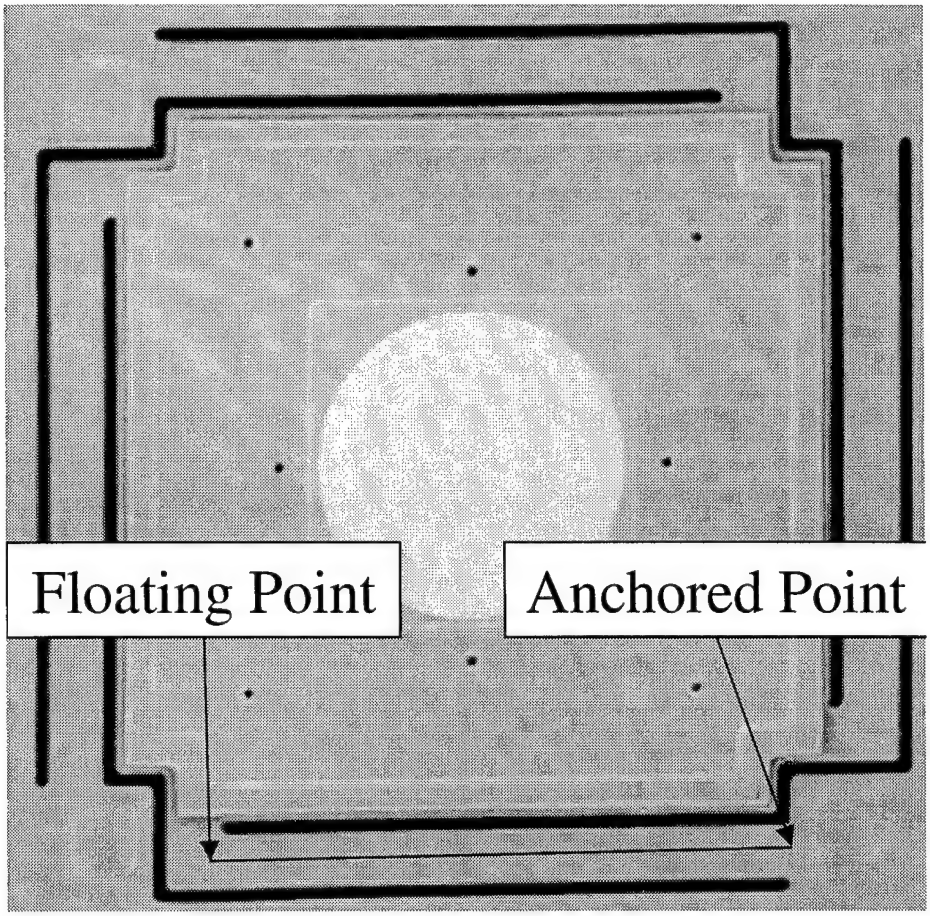


Figure 5-1. Measurement Height Contour Path [6].

A baseline measurement of the FBMD is needed to perform analysis of both the static and pulse width modulated performance. An HP6624A Power Supply provides the control voltage to the FBMD. Three measurements per control voltage are averaged by the Zygo to reduce the system noise error. Many measurements are made as the control voltage is varied between zero and the snap-down voltage[10]. After the static measurements are made, the HP6624A is replaced with the PWM16 ISA card, shown in

[10] Snap-down voltage – voltage at which the mirror's position becomes unstable. At and above the snap-down voltage, the mirror will fully deflect and "snap down" to the underlying electrode [6].

Appendix D. A simple transistor high-voltage switch is used to gate each output channel and amplify the output voltage, as shown in Figure 5-2.

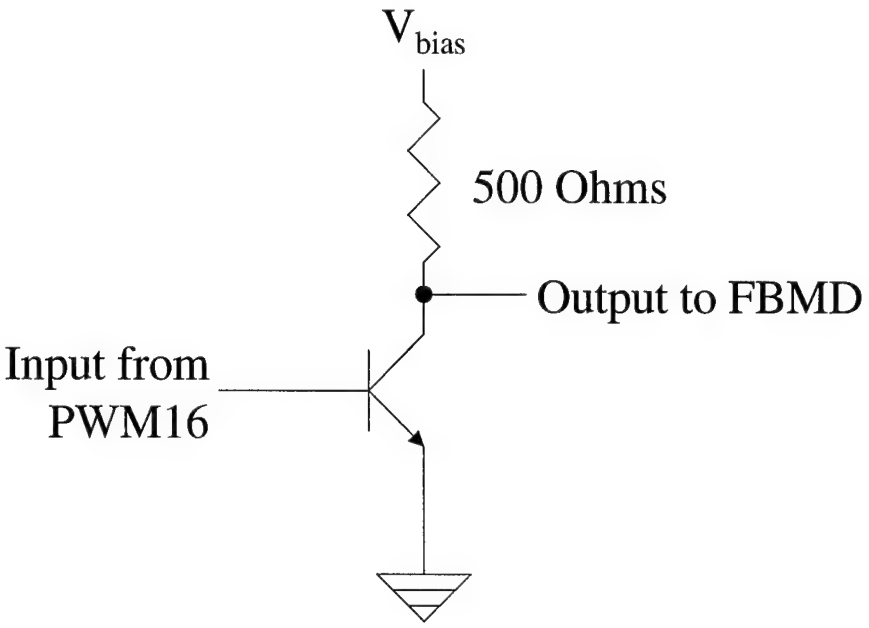


Figure 5-2. Transistor Output Switch.

V_{bias} is set to any voltage greater than the snap-down voltage and less than the V_{cemax} voltage of the transistor. The deflection of the FBMD voltage as a function of the V_{rms} at the output of the transistor switch is measured with an oscilloscope while using the PWM16 with transistor switch as the control voltage. Again, many measurements are many while varying the duty cycle of the pulse width modulated control voltage from zero until the mirror exhibits the "snap-through instability" [6].

5.4 Summary

The experiments presented in this Chapter are used to investigate the proper operation and to demonstrate the mirror deflection modulation capability of the controller. The experiments described in Section 5.2.1 enable a reduction of the effort necessary to troubleshoot a faulty system by providing a preliminary inspection of the chip which will detect many catastrophic failure mechanisms, such as incorrect wafer-to-carrier alignment or bonding, foreign material which could conduct between electrically isolated conductors, and shorted power and ground supply pins. The use of design-for-testability features allows the COUNT portion of the design to be fully exercised and verified separately from the overall operation of the design, as described in Section 5.2.2. The entire design is verified if the COUNT portion of the design is operational. Section 5.2.3 describes the experiment to investigate the operation of the remaining functional blocks of the design.

The correct operation of the design does not conclude the design testing. The design must emulate the response of an FBMD to a DC control voltage. A baseline set of measurement using a DC power supply and the corresponding measurements using the PWM16 are taken using the procedure described in Section 5.3. Chapter 6 includes the results and analysis of these experiments.

6 Results and Analysis

6.1 Introduction

The experiments described in Chapter 5 were performed, and the results were recorded and analyzed. The results of the experiments are detailed in Section 5.2.1 and the resultant corrective action is described in Section 6.2. The functional operation of the pulse width modulation controller, PWM16, as described by Sections 5.2.2 and 5.2.3, is reported in Section 6.3. A comparison of the theoretical and static DC deflection measurements explained in Section 5.3 and an analysis of the theoretical parameter calculations described in Section 2.3 are presented in Section 6.4. Section 6.5 includes the results of the pulse width modulation experiments described in Section 5.3. Finally, the comparison of the static DC and pulse width modulation measurements described in Section 5.3 were analyzed and are presented in Section 6.6.

6.2 Results of the Fabrication Inspection Experiment

The fabrication inspection experiment described in Section 5.2.1 was performed and exposed a serious design flaw. The visual inspection of the design confirmed that the wafer was oriented and bonded as specified. However the resistivity check found a virtual short between the power and ground supply pins. Referring to the original design file (see Appendix C), the upper left-hand power supply pad was found to be connected to a grounded guard ring. Figure 6-1 shows a zoomed view of the original layout with the problem areas highlighted. These areas were cut away using a laser cutter [25].

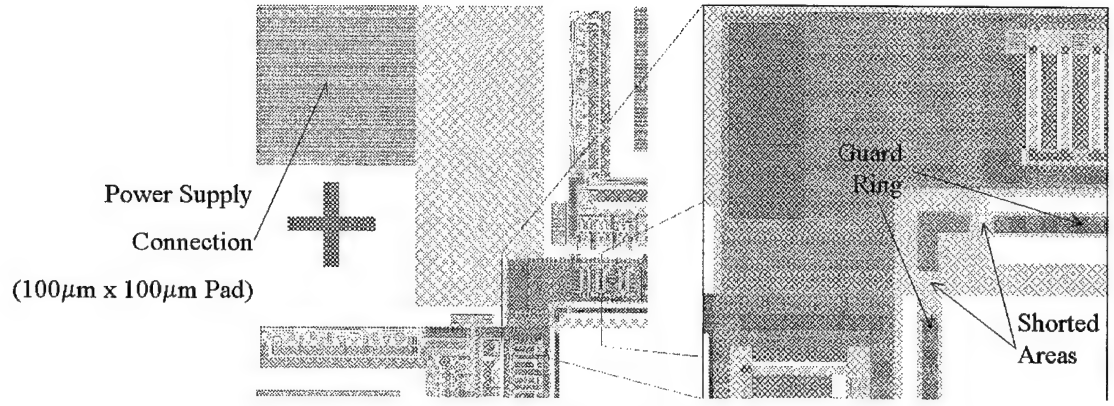


Figure 6-1. Shorted Power Pad Layout.

The resistance measurements were repeated after the laser-cut modification. All resistances between the power pins and ground pins were too large to be accurately measured with a two-wire resistance measurement. All reverse-biased resistances from ground pins to power pins were approximately 300 kΩ, which is consistent with the embedded diode protection system.

6.3 PWM16 Verification Experiment Results

The PWM16 COUNT verification experiment discussed in Section 5.2.2 was performed after the modification described in Section 6.2. The PWM16 was stimulated as described in Section 5.2.2 using a 10 MHz CLOCK signal and input stimuli provided by the HP82000 [23]. The output was verified using the HP82000. The PWM16 performed as expected.

The OUTPUT signal verification experiment depicted in Section 5.2.3 was performed with a single PWM16 connected as specified by the schematic in Appendix D and controlled with the software in Appendix E. The CLOCK signal was connected to

the 14.3 MHz OSC signal from the ISA bus of an IBM-compatible PC. All sixteen OUTPUTs were verified using an oscilloscope. Although the duty cycles of the OUTPUTs were correct, the open-circuit waveform deviated from the theoretical waveform shown in Figure 2-14. The rise and tall times, identified as T_{rise} and T_{fall} respectively, are dependent upon the actual high-voltage switch transistor and the supply voltage V_{bias}. The rise and fall times were approximately 140 ns and 210 ns, respectively when using an RCA SK3550 transistor and a V_{bias} of 20 volts. When the duty cycle was near zero, the rise and fall times were longer than the duty cycle time. A zoomed section of the triangular waveform that was observed when the sum of the rise and fall times were greater than the applied duty cycle time is shown in Figure 6-2. Notice that the peak of the triangular waveform was less than V_{on}.

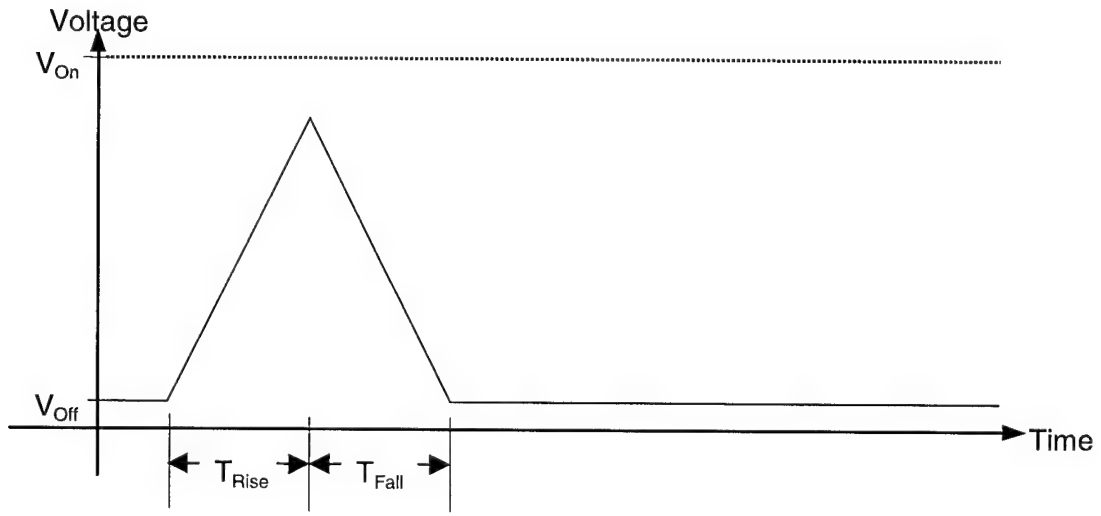


Figure 6-2. Triangular Waveform.

As the duty cycle increased, the waveform changed from a triangular waveform to a trapezoidal waveform. The sum of the rise and fall times were no longer greater than the

duty cycle times, but were of the same order of magnitude, as shown in Figure 6-3. The effect of the trapezoidal waveform decreased as the duty cycle increased, until the duty cycle time was much larger than the sum of the rise and fall times. The square wave model presented in Figure 2-14 was then approximated until the duty cycle was sufficiently large, approximately ninety-five percent. The effects at the upper end of the duty cycle were an inverse effect of the trapezoidal and triangular waveforms caused by the significance of the fall and rise times, as expected.

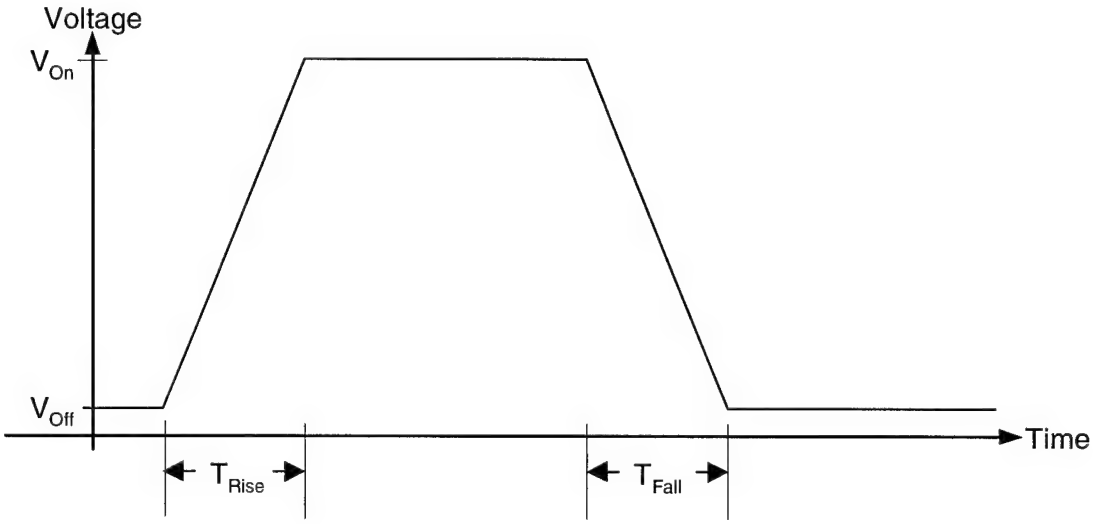


Figure 6-3. Trapezoidal Waveform.

6.4 Static FBMD Operation

The static DC operation experiment presented in Section 5-4 was performed following the OUTPUT verification described in Section 6.3. The resonant frequency analysis from Section 2.7 predicted that the 10 μm-width flexure FBMD would have the

highest resonant frequency, which would cause it to be the most difficult to control of all six FBMD designs. Using Equation (2-3), the geometry of the 10 μm-width flexure FBMD, and the Poly1 material properties listed in Table 6-1, k simplified to 31 N/m.

Table 6-1. Material Properties for MUMPs 23 Design [13, 26].

E, modulus of Elasticity	σ, residual stress	υ, Poisson ration	t, thickness of Poly1	$Z_{resting}$, thickness of Oxide1
160 GPa	6 MPa (Compressive)	0.22	1939.2 nm	1989.3 nm

The separation between the flexure and the underlying electrode, defined as the resting height of the FBMD $Z_{resting}$, was determined by the thickness of Oxide1. The Oxide1 thickness was provided by the fabrication service and is listed in Table 6-1. Using the information in Table 6-1, Equation (2-6) simplified to:

$$V = (1989.3nm - Deflection) \cdot 3.0299 \cdot 10^{9} \cdot \sqrt{k \cdot Deflection} \qquad (6\text{-}1)$$

Substituting the previously computed k into Equation (6-1) yielded:

$$V = (1989.3nm - Deflection) \cdot 1.7376 * 10^{10} \cdot \sqrt{Deflection} \qquad (6\text{-}2)$$

The theoretical voltage versus deflection and the measured values taken using a MUMPs 23 10 μm-width flexure FBMD are plotted in Figure 6-4. A tabular representation of data shown in Figure 6-4 is contained in Appendix F.

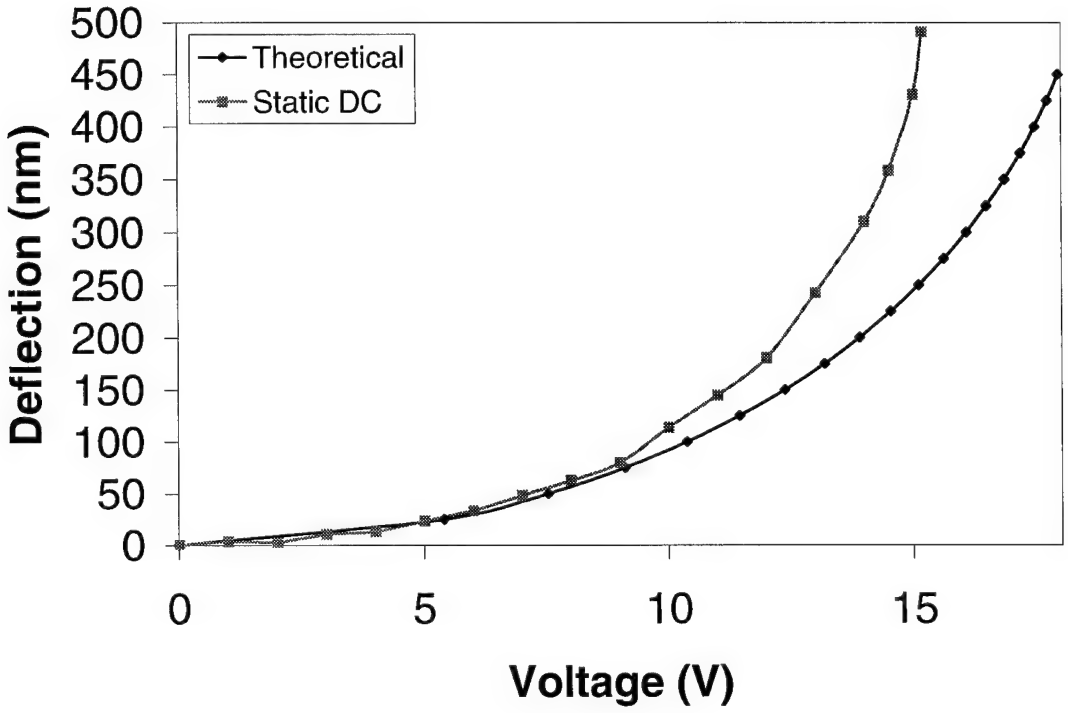


Figure 6-4. Voltage vs. Deflection for 10 μm-Width Flexure FBMD.

There was significant error between the theoretical and measured values. This error was due to an incorrect spring constant *k* calculation resulting from typical run-to-run deposited material variations in the MUMPs process and deviations of the actual thin-film parameters from published parameters. The standard approach to correct for this error is to extract a *k* value from the measured data [6]. Equation (6-1) described the relationship of the voltage *V*, *Deflection*, and the spring constant *k*. The spring constant *k* was calculated at each voltage versus deflection point using the measurements from the static DC experiment results (see Appendix F). The spring constant as a function of voltage is plotted in Figure 6-5. A spring constant *k* of 26 N/m was chosen as the best fit

for the data and is shown in Figure 6-5. The error between the measure and calculated spring constant was 22%, which is typical of the MUMPs process [6].

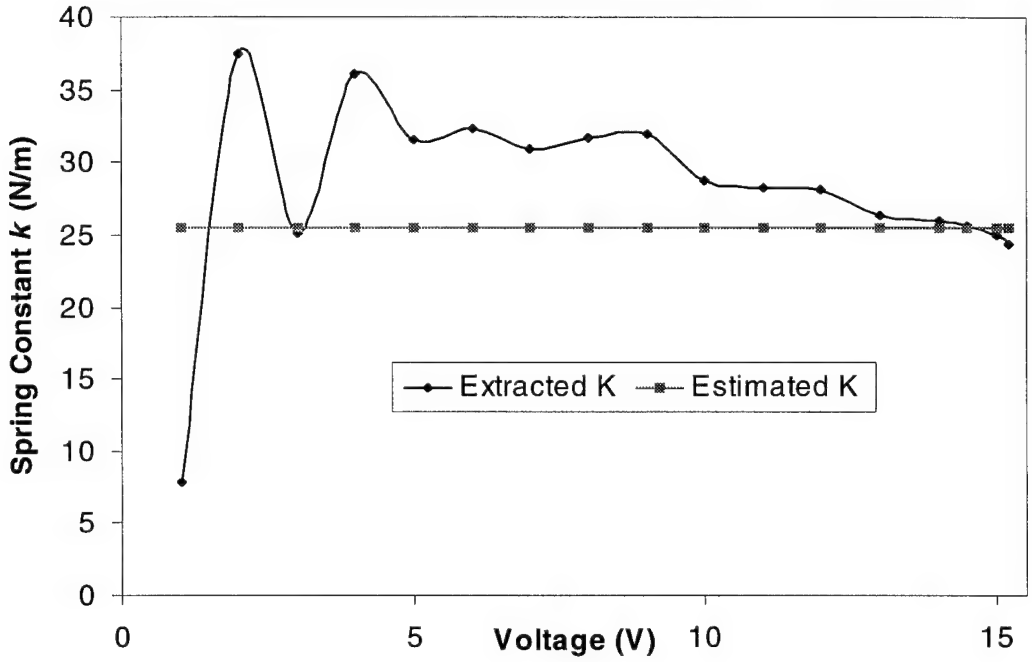


Figure 6-5. Spring Constant k vs. Voltage for 10 μm-Width Flexure FBMD.

The theoretical FBMD response was recalculated using the new spring constant k of 26 N/m. Figure 6-6 shows a good agreement between the recalculated theoretical and measured static DC deflections as a function of voltage [27]. However, at the upper range of deflection, the static DC measured deflections deviated from the theoretical values. This deviation is characteristic of the simple model used. The sources of such model deviations are device dependent. With large square mirrors, which included the mirrors used in this research, the primary sources of error are speculated to be surface deformation and mirror elasticity [2]. However, the model in Equation (6-2) and the resulting graph in Figure 6-6 give a sufficient approximation of the voltage to deflection relationship.

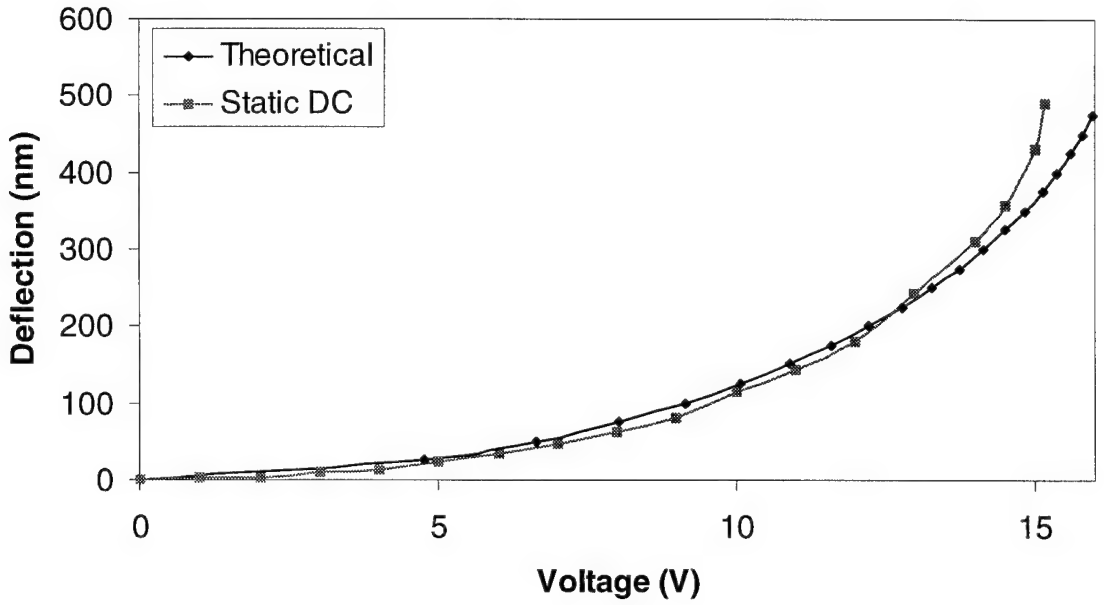


Figure 6-6. Theoretical and Measured Voltage versus Deflection for 10 μm-Width Flexure FBMD using the Spring Constant k = 26 N/m Based on Measurements.

6.5 Pulse Width Modulated FBMD Operation

The deflection as a function of voltage experiment presented in Section 6.4 was repeated using the PWM16. The ISA card used to verify the functionality of the OUTPUTs, as described in Section 6.3, was used with the transistor high-voltage switch shown in Figure 5-2. The root-mean-square voltage, V_{rms}, at the collector of the transistor was theoretically calculated based upon Equation (2-9). However, Equation (2-9) described a continuously variable duty cycle and the "on" and "off" voltage as variables, V_{on} and V_{off} respectively. V_{on} was equal to the supply voltage V_{bias}, since the electrostatic actuation mechanism of the FBMD required negligible current. The static DC deflection measurements described in Section 6.4 determined that the "snap-down" voltage was

approximately 15.2 volts. V_{bias} was chosen to be 20.0 volts to ensure that a full range of deflections up to and including "snap-down" could be measured. The collector-to-emitter voltage of the transistor in saturation determined V_{off}, which was measured as 0.4 volts. Equation (2-9) was simplified to account for the discrete duty cycle, the 14.3 MHz CLOCK, and the specific voltages V_{on} and V_{off}, as shown in Equation (6-1).

$$Vrms = \sqrt{1.50 \cdot DutyCycleNumber + 0.16} \tag{6-1}$$

The calculated V_{rms} agreed well with the measured V_{rms} for most duty cycle values. However, as described in Section 6.3, the low and high duty cycle values, approximately 6% and 95%, deviated from the ideal waveform used to derive Equation (6-1). The actual V_{rms} of the control voltage was measured for each duty cycle value to more accurately compare deflections produced with pulse width modulated V_{rms} values and static DC voltages. The duty cycle value was varied so that V_{rms} would range in approximately one volt increments from zero to the "snap-down" voltage. Figure 6-7 compares the pulse width modulated measurement, taken with V_{bias} equal to 20 volts, to the static measurement displayed previously.

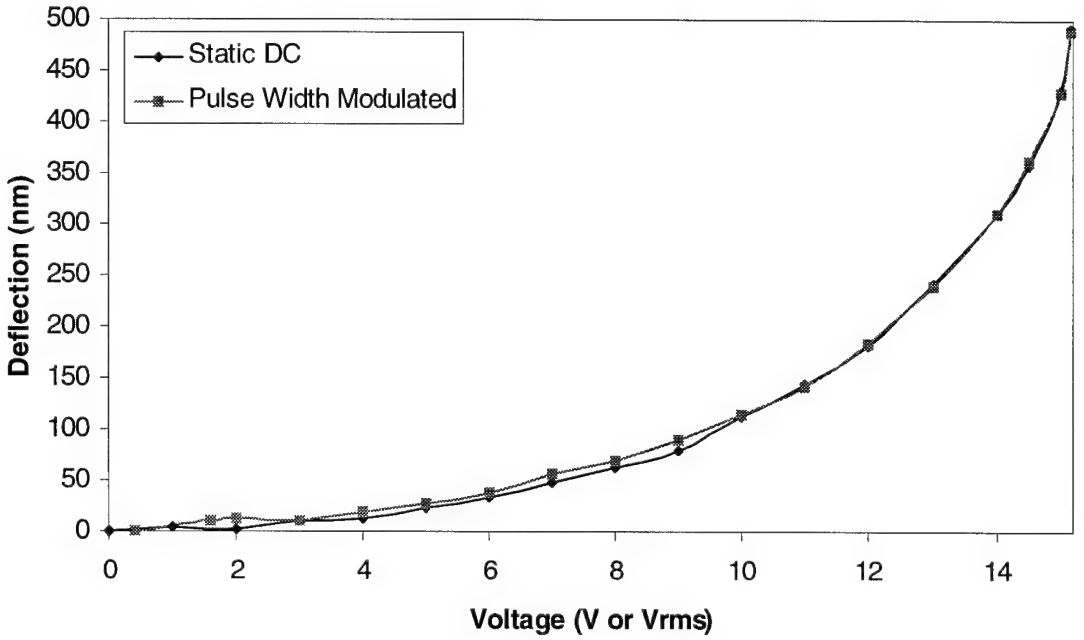


Figure 6-7. Comparison of Static DC and Pulse Width Modulated Control Voltage vs. Deflection for 10 μm-Width Flexure FBMD.

6.6 Measurement Error and Result Analysis

The results of the measurements, reported in Sections 6.4 and 6.5, were used to determine the performance of the controller. Both sets of measurements included the error induced by the equipment operator and the limitation of the test setup. Section 5.3 described the method used to record the deflection. A maximum difference in height along a line defined by two points, the floating point and the anchor point (see Figure 5-1) was defined as the measure of deflection. Both the floating point and the anchor point were defined using the topology of the flexure. Gaps in the POLY0 under the flexure caused depressions on the surface of the flexure, which were used as references for the endpoints of the contour path. Both endpoints were defined using a cursor that

was graphically manipulated after each measurement. The Zygo software did not allow the scan line to be saved between measurements. The selection of the both endpoints and the resolution limitations of the cursor restricted the accuracy of the measurements, ± 2.5 nm. Summing the possible error between the two sets of measurements resulted in a 10 nm height variation allowance. The differences between the static DC and pulse width modulation measurements was less than the 10 nm allowable variation. In addition, the standard deviation in the error recorded between the two sets of measurements was 3.0 nm. The actual deviation and the standard deviation are shown in Figure 6-8. Appendix F and G list the actual measurements made.

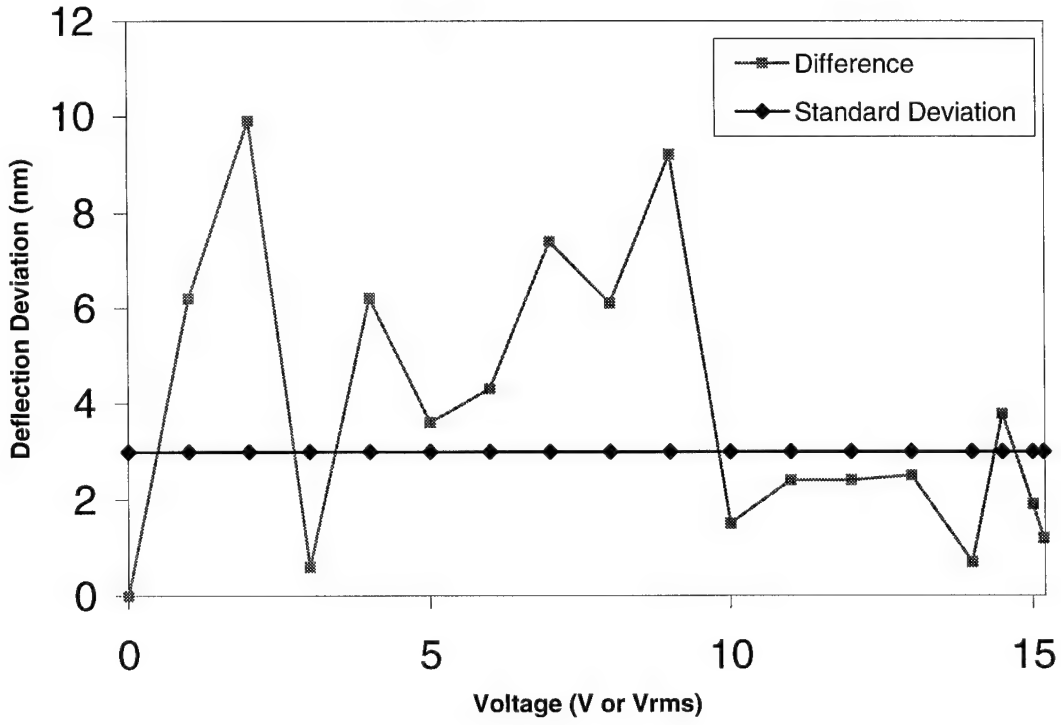


Figure 6-8. Deviations of Static DC and Pulse Width Modulated Deflection Measurements vs. Control Voltage for 10 μm-Width Flexure FBMD.

6.7 Summary

The PWM16 was capable of controlling the FBMD. However, the initial as-fabricated design contained two shorted nodes. Fortunately, these nodes were repairable with laser modification. These problems and the associated solutions are found in Section 6.2.

The PWM16 was functionally verified using two procedures, as described in Section 6.3. The PWM16 operated correctly throughout the entire range of duty cycles, from 0% to 99.6% at 14.3 MHz. However, output waveform anomalies were observed under at the extremes of the duty cycle range, less than 6% and greater than 93%. A discussion of the output waveform variations are present in Section 6.3.

The deflection measurement results taken as specified in the experiments of Section 5.3 are reported in Sections 6.4 and 6.5. Deviations from the theoretical model were observed. A new spring constant k was extracted from the static DC measurements. The static DC measurements agreed well with the theoretical model when the extracted spring constant k was applied. The differences between the pulse width modulated and static DC deflection measurements were less than the noise margin of the test setup, as analyzed in Section 6.6. This analysis supports the conclusion that the PWM16 controls the deflection of FBMD with extreme accuracy.

7 Summary and Conclusions

7.1 Summary

This research illustrates the analysis and operational modeling necessary to control a device using pulse width modulation. Electrostatically-actuated, piston-action flexure beam mirror devices (FBMDs) exemplify a common microelectromechanical system (MEMS) device. FBMDs are used to illustrate the design criteria of the modulation controller. The analysis of the design includes the deflection versus voltage function and the frequency response model of the device. The advantages of using pulse width modulation over other voltage regulation methods are also covered.

Block diagrams and gate-level schematics presented in this research describe the implementation of a pulse width modulation controller capable of controlling multiple devices of varying types and/or sizes. The controller is capable of a duty cycle range from 0% to 99.6%. However, the rise and fall times of the output waveform distort the square waveform at the upper and lower extremes of the duty cycle.

The results of the experiments show a good agreement between the theoretical model, using an extracted spring constant k, and the static DC deflection measurements. In addition, the pulse width modulation measurements almost identically agree with the static DC measurements. These experiments and results of these experiments demonstrate that the pulse width modulation controller is capable of controlling FBMDs to within the noise margin of the test setup.

7.2 Conclusion

This thesis demonstates pulse width modulation at an update frequency greater than the highest resonant frequency of the FBMDs in a given will control the deflection of all MEMS mirrors in the system with the same degree of measured accuracy as an analog control voltage. The accuracy of the measurements was limited by the test fixture to 5 nm per measurement.

The pulse width modulation method, as implemented in the complimentary metal oxide semiconductor (CMOS) controller PWM16, is superior to the current state-of-the-art control system [7]. The PWM16 is more cost-effective than a computer-controlled variable voltage power supply or the current multi-channel digital-to-analog converters (DACs). In addition, the control system, as implemented with the PWM16, is more compatible with a higher level of integration than a multi-channel DAC based controller design. The required effort necessary to increase the level of integration is described in Section 7.3.

7.3 Areas for Further Research

Although this research investigated all proposed areas of interest, other research interests became evident during the course of this work. Section 7.3.1 describes the incorporation of application-specific input and output pad modifications. Section 7.3.2 covers a proposed increase in the level of integration. Section 7.3.3 illustrates two possible application-specific mirror effects that could occur when using the pulse width modulation controller.

7.3.1 Input and Output Pad Replacement

The digital CMOS-compatible input and output pads were supplied by MOSIS [16] and chosen for their design maturity. The input pads of the controller are compatible with a 5-volt CMOS microprocessor. If a different technology microprocessor is chosen to interface to the controller, the input pads should be changed to be directly compatible without a logic level conversion. These pads are as follows: DATA bus, ADDRESS bus, TEST, CLOCK, STROBE, and RESET. For example, the schematic shown in Appendix D uses HCT logic to interface between the TTL signals of the ISA bus and the 5-volt CMOS inputs of the controller [28].

The digital CMOS-compatible output pads of the controller provide only a limited range of deflections. Referring to Figure 6-6, a 5-volt control voltage provides approximately 24 nm of deflection for the 10 μm flexure width FBMD. An output voltage shift circuit shown in Figure 5-2 should be incorporated into the output pad of the controller. In addition, since the output load of the FBMD is entirely capacitive, a charge pumping design could be constructed to increase a single supply voltage. For example, a circuit that tripled a 5-volt power supply for the logic would provide sufficient output voltage to control the 10 μm FBMD to close to the "snap-down" [6] voltage.

7.3.2 Level of Integration

The modulation system with FBMD, as presented in this research, exhibits a very low level of integration. The controller was fabricated and packaged separately from the FBMDs, and additional output voltage-level shifting and input logic-level shifting were achieved externally. Section 7.3.1 discusses the necessary changes to the input and

output pads. A more integrated packaging of the controller and FBMD would produce a lower-weight, lower-system floorspace, and higher performance design if the previously described change are made.

7.3.3 Mirror Effects

All experiments presented in this research were performed on a single mirror within an array. Previous research shows that cross-talk between mirror elements is non-existent or negligible for devices similar to those used in this research. However, these measurements were taken at below resonant frequencies [2]. No cross-talk effects using the modulation method presented in this thesis are predicted. However, if control of devices different than those presented in this thesis is desired, the cross-talk effects should be verified for the intended devices.

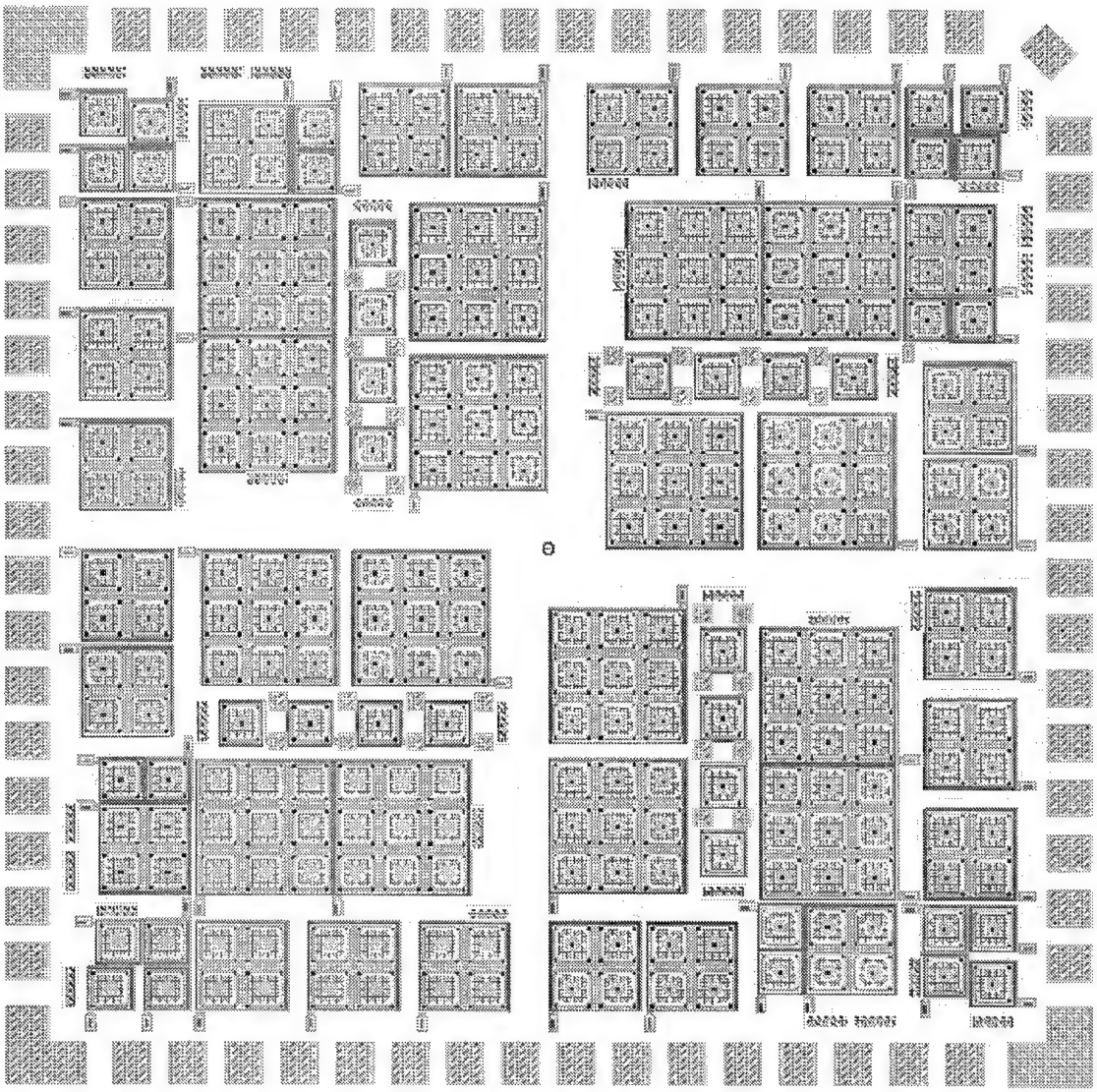
In addition to cross-talk effects, the "snap-down" effect of a static DC voltage controlled electrostatic mirror limit the usable deflection range of the FBMD to approximately one third the resting height, see Figure 2-3. Using the pulse width modulation method, the stable range of the mirror deflection may be increased.

Appendix A – Surface Micromachining Release Processing

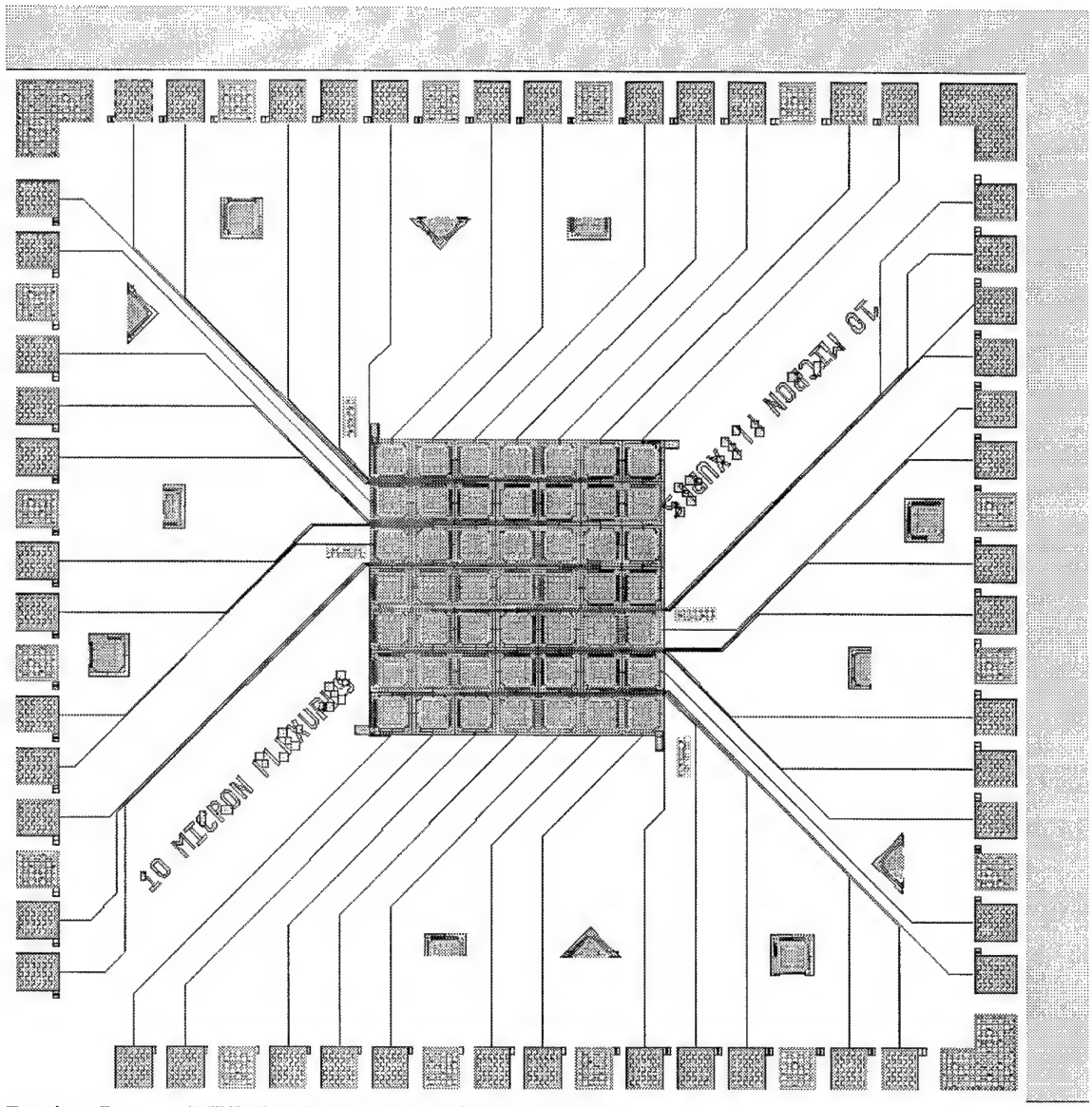
The following procedures describe the post-fabrication processing. This processing includes both the release etch and wafer packaging.

1. Clean all containers with acetone and liquid nitrogen.
2. Label containers as: First Methanol, Second Methanol, First Acetone, Last Acetone, and hydrofluoric acid (HF).
3. Fill all containers with appropriate chemicals. Use only fresh chemicals.
4. Place wafer carrier on 150 °C hot plate.
5. When wafer carrier reaches temperature, apply CrystalBond 509 to wafer carrier.
6. Align die with wafer carrier and place die in the wafer carrier. Remove wafer carrier from hot plate and allow to cool.
7. To remove the bulk of the photoresist, submerge the device in First Acetone. Place device with die facing upward to ensure the die remains bonded to the carrier. Leave submerged 10 minutes.
8. To finish removing any residual photoresist, move device to Last Acetone and repeat placement instructions from step 7. Leave submerged 10 minutes.
9. To remove the acetone, place device in First Methanol. Leave submerged 5 minutes.
10. To perform the release etch, submerge the device in HF. The etch time is design specific. FBMD mirrors are released after 3 minutes. Leaving the device in HF for a longer than 3 minutes is detrimental to the polysilicon.
11. To remove the HF, submerge device in First Methanol for 5 minutes.
12. To finish removal of HF, submerge device in Last Methanol for 10 minutes.
13. Place device on 55 °C hot plate to dry.
14. Wirebond electrical connections between die and wafer carrier.
15. Store in a dry area using a desiccant, if possible.

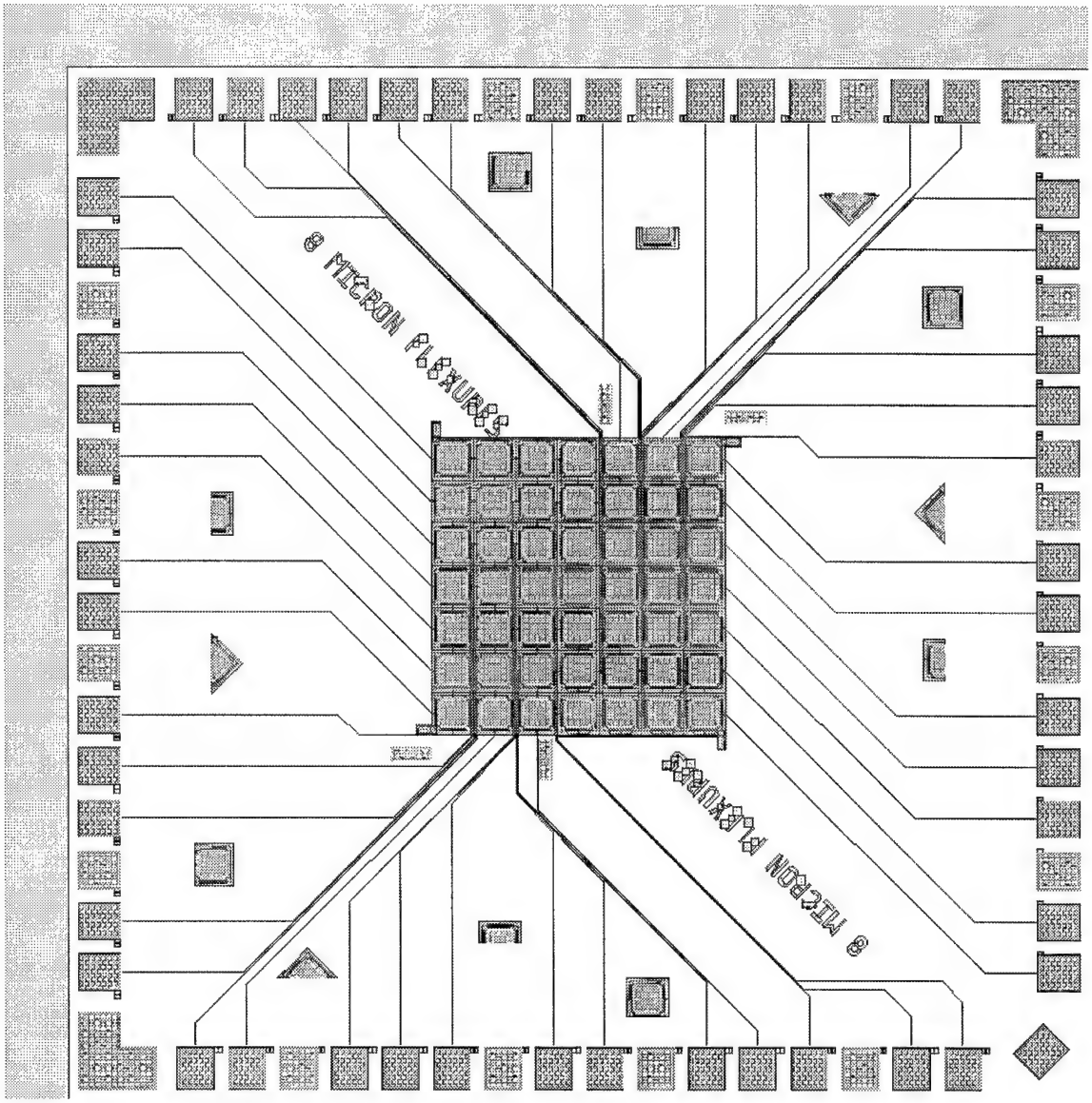
Appendix B – FBMD Designs



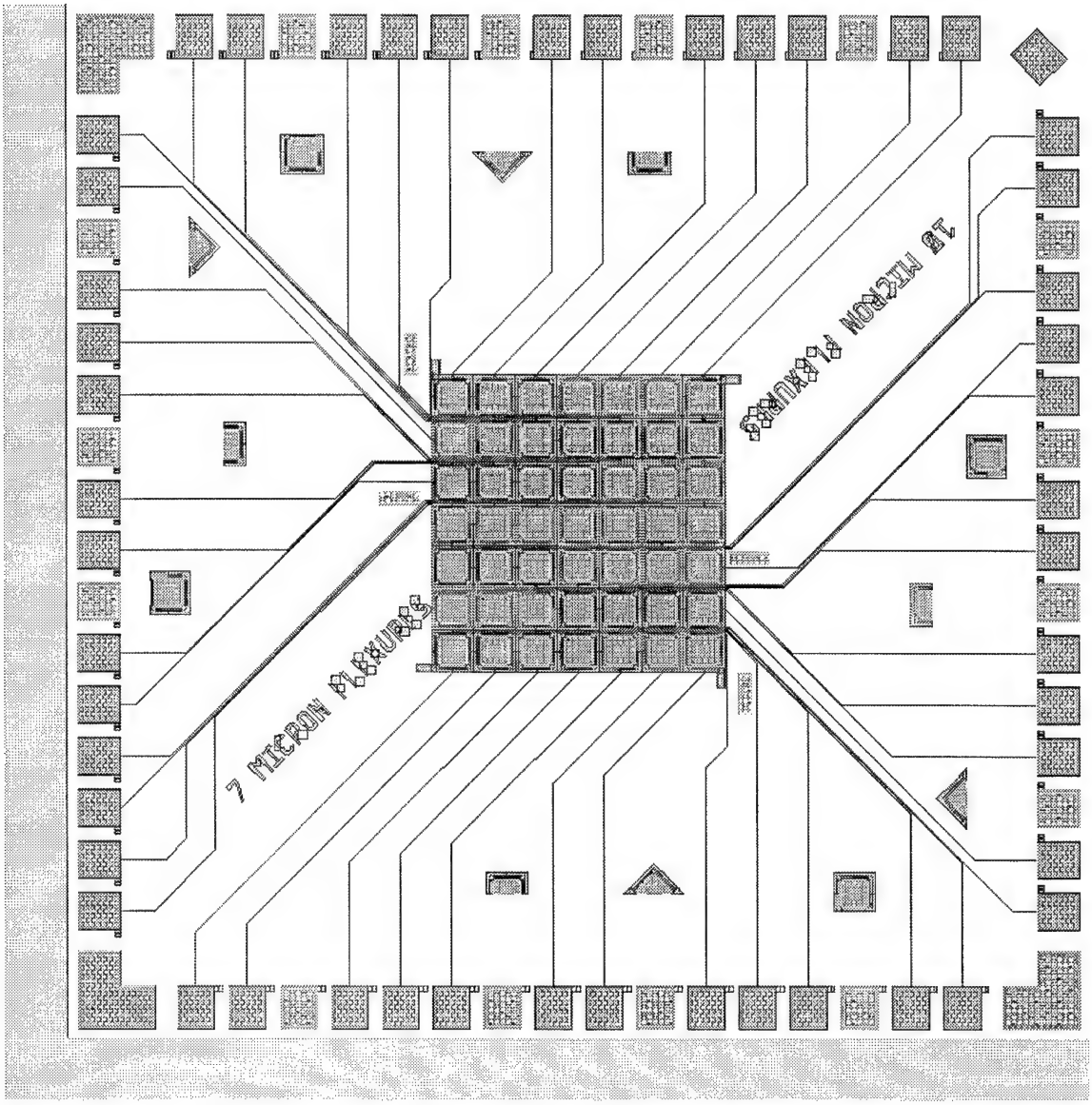
Design Run: MUMPs 22
Purpose: Frequency verification of mirrors and mirror arrays using the laser interferometer
Packaging: None (68 Pin PLCC package pad frame)
Size: Quarter die
Comments: Design placed as many mirrors as possible on one quarter die. Mirror flexure widths range from 5 μm to 10 μm. Mirrors range from single elements to 3x3 arrays.



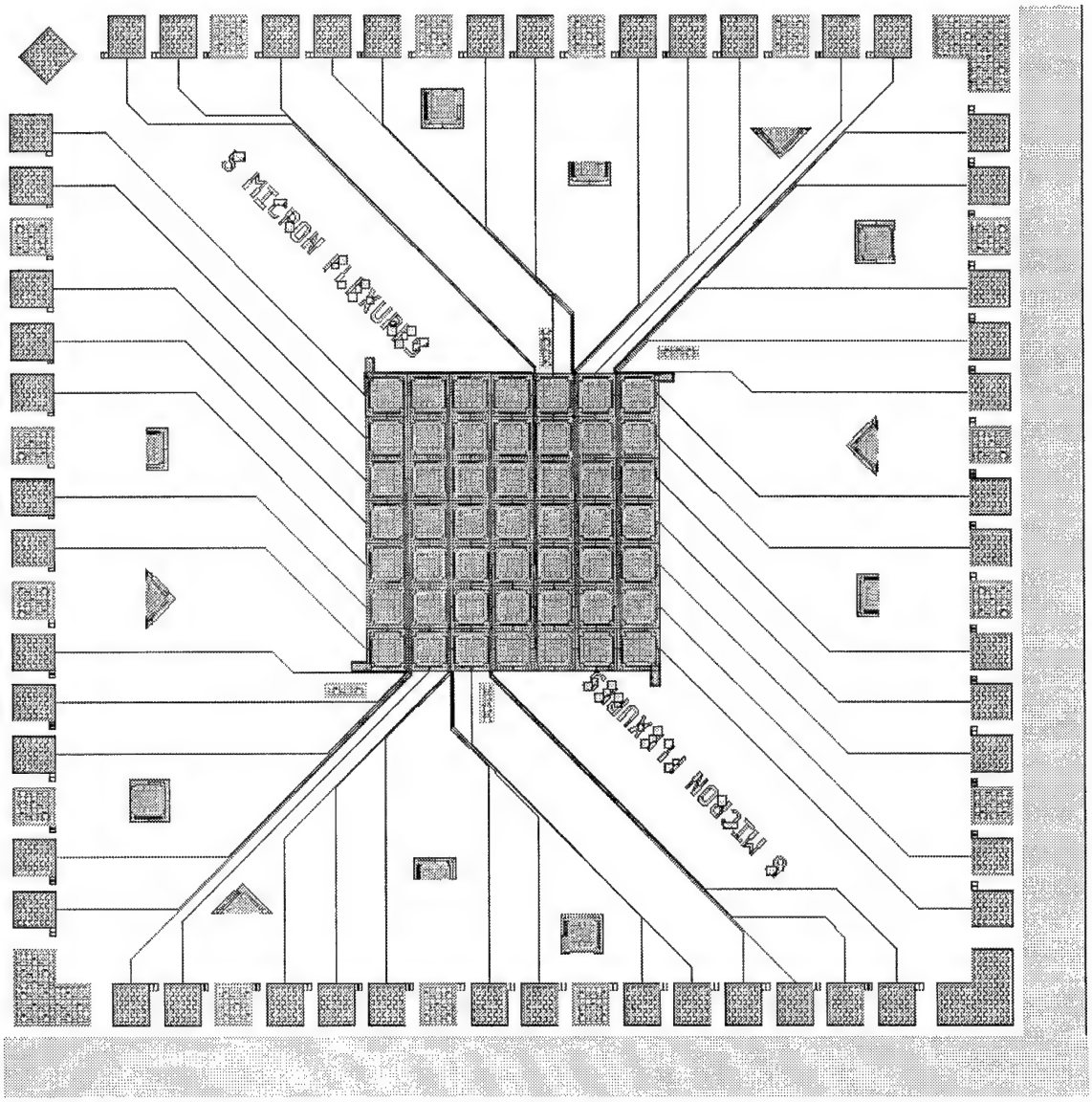
Design Run: MUMPs 23 Lower Left Quarter Die
Purpose: Pulse Width Modulation verification of mirrors using the Zygo
Packaging: 68 Pin PLCC
Size: Quarter die
Comments: 7x7 10 μm Flexure Width FBMD Array



Design Run: MUMPs 23 Lower Right Quarter Die
Purpose: Pulse Width Modulation verification of mirrors using the Zygo
Packaging: 68 Pin PLCC
Size: Quarter die
Comments: 7x7 8 μm Flexure Width FBMD Array

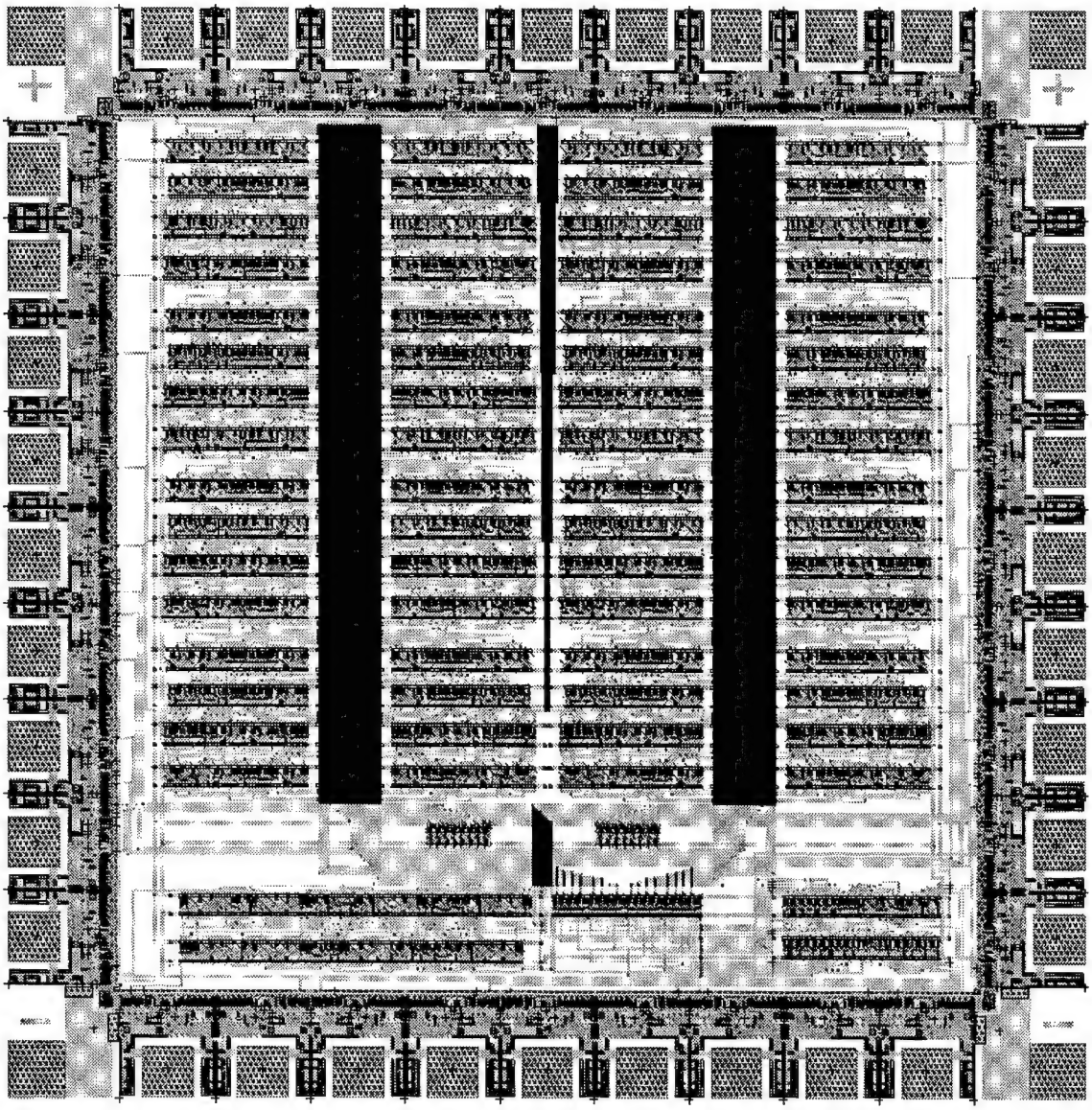


Design Run: MUMPs 23 Upper Right Quarter Die
Purpose: Pulse Width Modulation verification of mirrors using the Zygo
Packaging: 68 Pin PLCC
Size: Quarter die
Comments: 7x7 7 μm Flexure Width FBMD Array

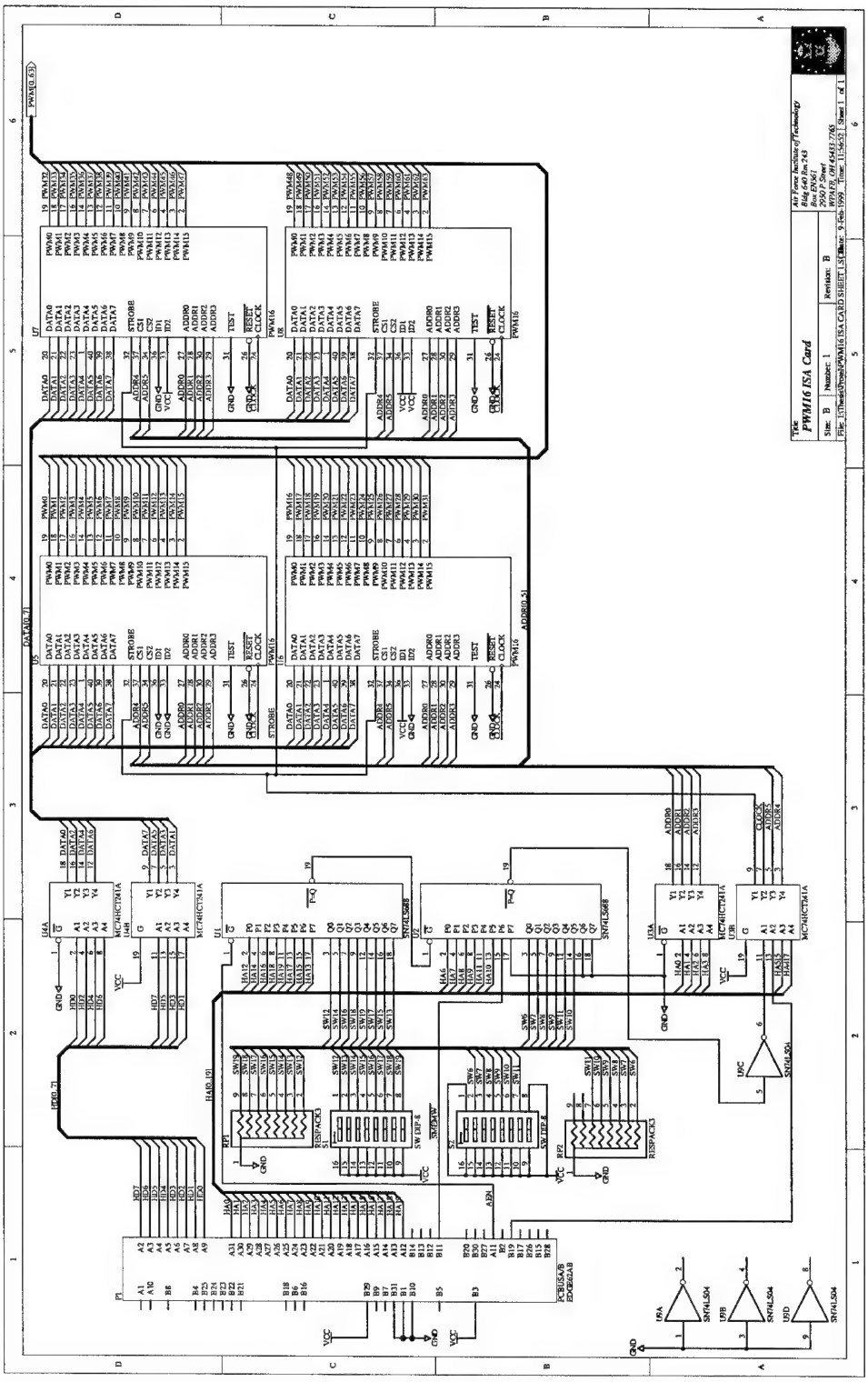


Design Run: MUMPs 23 Upper Left Quarter Die
Purpose: Pulse Width Modulation verification of mirrors using the Zygo
Packaging: 68 Pin PLCC
Size: Quarter die
Comments: 7x7 5 μm Flexure Width FBMD Array

Appendix C – PWM16 Design Layout



Appendix D – PWM16 ISA Card Schematic



Appendix E – PWM16 ISA Card Software

```
#include <stdio.h>
#include <stdlib.h>
#include <dos.h>

#define MAXMEM 16
#define BASEADDR 0xd000

int main()
{
      unsigned char far *ucData;     // Pointer to Card
      int iPWM;                      // PWM channel index looper
      int iData;                     // Duty cycle looper

      // Make pointer to base address of card
      // Address card by ucData[PWM #] = Duty Cycle
      ucData = (unsigned char *) MK_FP (BASEADDR,0000);

      // Step 1
      // Reset all 16 channels starting at channel 0
      for (iPWM = 0; iPWM < MAXMEM; iPWM++)
            ucData[iPWM] = 0;

      // Step 2
      // Loop through all 16 channels starting at channel 0
      for (iPWM = 0; iPWM < 16; iPWM++)
            // Loop through all 256 duty cycles starting with 0
            for (iData = 0; iData < 257; iData++)
            {
                  // Step 3
                  // Write duty cycle to output channel
                  ucData[iPWM] = (unsigned char) iData;

                  // Step 4
                  // Print current status
                  printf ("Output channel %d = %d\n",iPWM, iData);

                  // Step 5
                  // Wait for key press to increment duty cycle
                  if (getch() == 3)
                        return 0;

                  // Step 6
                  // Repeat until zero (256)
            }
            // Step 7
            // If output channel pointer is not equal to last output
            // channel, increment output channel pointer and repeat
      // Step 8
      // End routine
      return 0;
}
```

Appendix F – Measurements of Static DC Deflection

The following results were taken using the Zygo laser interferometer, the HP6624A Power Supply, and a 10 μm flexure width FBMD. Although the Zygo has a measurement accuracy of 0.3 nm, the measurements take are the difference between two point and are limited to the graphic resolution of the cursor (see Section 6.6).

Voltage (V)	Deflection (nm)
0.0	0.0
1.0	3.7
2.0	3.1
3.0	10.5
4.0	13.0
5.0	23.5
6.0	33.4
7.0	48.2
8.0	62.5
9.0	79.8
10.0	113.5
11.0	144.6
12.0	180.5
13.0	242.3
14.0	310.3
14.5	358.5
15.0	430.8
15.2	490.7

Appendix G – Measurements of Pulse Width Modulated Deflection

The following results were taken using the Zygo laser interferometer, the HP6624A Power Supply, the PWM16 ISA Card (see Appendix D), the transistor voltage level shifter circuit (see Figure 5-2), and a 10 μm flexure width FBMD. The bias voltage was 20 volts. Although the Zygo has a measurement accuracy of 0.3 nm, the measurements take are the difference between two point and are limited to the graphic resolution of the cursor (see Section 6.6).

Voltage (V)	Deflection (nm)
0.4	0.0
1.6	9.9
2.0	13.0
3.0	11.1
4.0	19.2
5.0	27.1
6.0	37.7
7.0	55.6
8.0	68.6
9.0	89.0
10.0	115.0
11.0	142.2
12.0	182.9
13.0	239.8
14.0	309.6
14.5	362.3
15.0	428.9
15.2	489.5

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Vita

Captain Paul Corley Rounsavall was born on 21 August 1971 in Arlington, Texas. He graduated from Southern Baptist Educational Center in 1989. He accepted an Air Force ROTC scholarship at Detachment 425, Mississippi State University and graduated with a Bachelor of Science in Electrical Engineering degree on 15 December 1993. Following graduation, on 20 December 1993, he was commissioned a Second Lieutenant in the United States Air Force.

Captain Rounsavall's first assignment was to the Norman Oklahoma Next Generation Weather Radar (NEXRAD) Operational Support Facility. While at NEXRAD, he earned a Master of Business Administration degree from Oklahoma City University in June 1997. He was then selected to attend the Air Force Institute of Technology (AFIT) Wright-Patterson AFB, Ohio. He graduated from AFIT on 23 March 1999 with a Masters of Science Degree in Electrical Engineering. He is currently a doctoral student at AFIT in the Department of Electrical and Computer Engineering.

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